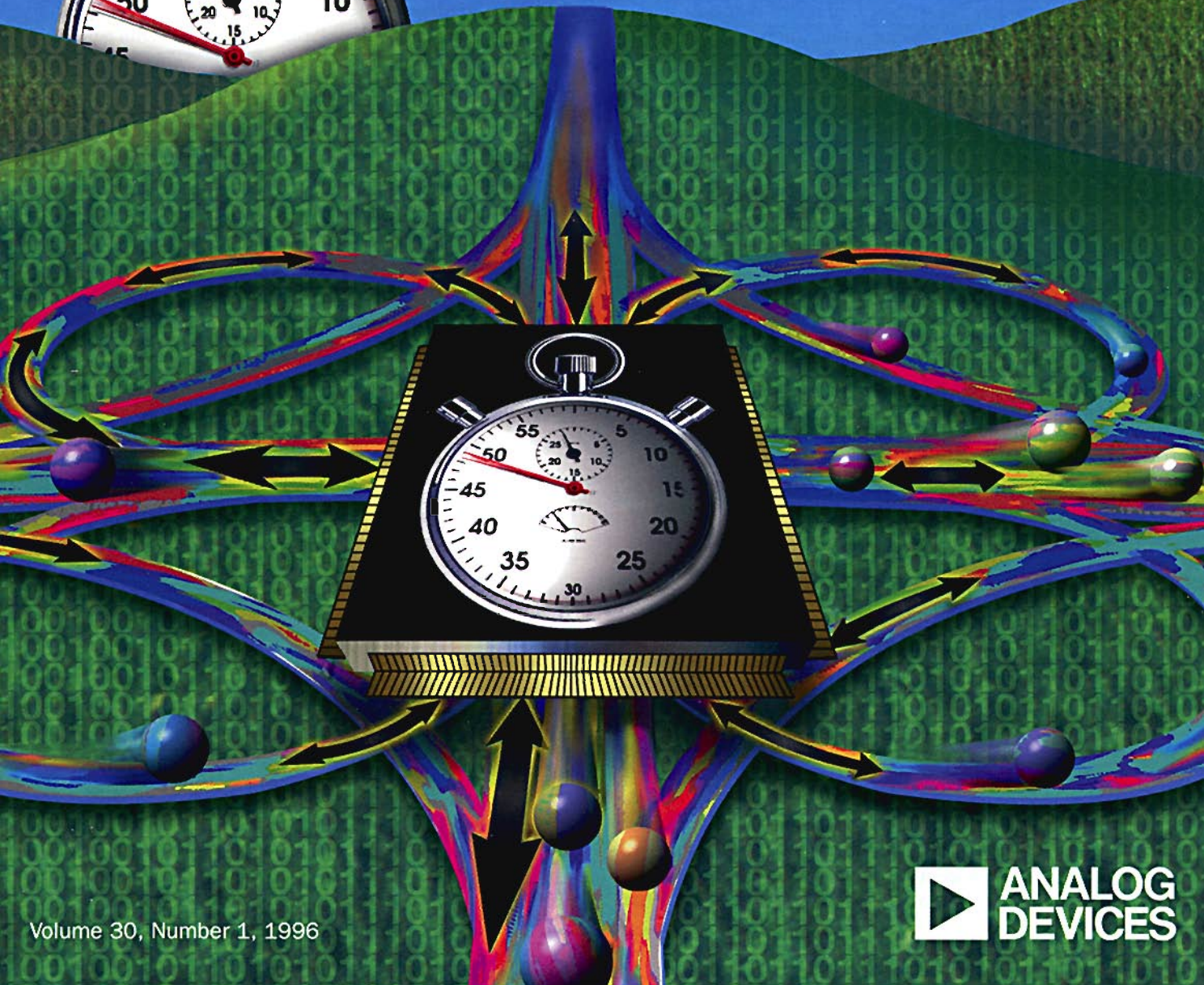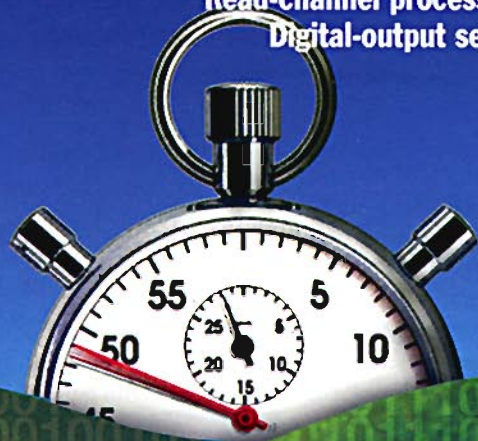# Analog Dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing

NEW DSP FOR HIGH-PERFORMANCE/CONCURRENT SIGNAL PROCESSING (page 6)

Read-channel processor uses PRML to increase disk-drive capacity (page 3)
Digital-output sensor simplifies temperature acquisition (page 12)

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ANALOG
DEVICES

Editor's Notes

THE COMPUTER EXPERIENCE

We just bought our third home personal computer. The first (1981) was an Apple II Plus with 16 K of RAM and a special plug-in card with all of 16 K additional (wow!), and a diskette drive that would handle about 143 K. The second (1990) was a Macintosh Classic with four MB of RAM and (about) 40 MB hard disk. The latest is a Mac Performa with a Power PC chip, 16 MB of RAM, a gigabyte of hard disk, a CD-ROM drive, 14.4 kb/s modem, and a color display—loaded with software and accompanied by a clutch of CD ROMs. It's interesting that *all three purchases made equal-size dents in the checkbook* (in then-current dollars).

Analog has historically been our personal forte. Before taking a byte out of our first Apple, the only programming we had attempted was in machine-language on a Heathkit µP trainer. So that first Apple provided a totally new experience. We learned to write Basic programs, actually wrote some useful programs, and concluded that the computer was basically a hardware "slave"—an entity that would obey all instructions that it was capable of recognizing. The challenge came in actually writing a program that was 100% recognizable and glitch-free, and could survive the endless nitpicking the computer was supremely capable of.

With the second computer, the word processors, spread-sheets, and drawing programs, etc.—and seemingly endless memory—made it possible to do lots of productive things. But the computer was no longer fun, it was a reliable everyday "tool". The challenges were gone. We got fat, dumb, and happy. Would a new, more-advanced computer further increase the convenience?

Perhaps. But the prime reason for buying the new computer was to add Internet access to our everyday capabilities, providing the increased speed and memory capacity needed to handle graphics. The first thing we found was that, in spite of all the capabilities mentioned in the first paragraph, *the challenges were back!* They taught us the real nature of the computer experience. Bringing up a new computer capability is *a set of games for sharpening human problem-solving abilities*—replete with wins, losses, frustrations and triumphs—while playing against the clock.

We logged in with a full-service on-line company, then headed for the Internet button. Oops! a dialogue box: Download the Web browser. After finding it and downloading, we headed for the Internet button. Oops! Now one must install a whole new set of the company's software—or so it would seem! Finally we got it right, trashing the old software, installing the new. At last we could watch Web graphics forming images at a glacial pace.

Later, to avoid astronomical billlings for time on the Internet, we signed up with an on-line company that provided service for a fixed monthly fee. During installation, we found three sources of instructions—a cover letter, a manual, and Read Me on disk—each suggesting some different settings. Before everything worked OK, there were long-distance phone calls to Technical Support, each with at least half-hour wait—and at one point a change of server. Each new hassle was a loss, getting it resolved was a win, and losing time was a huge frustration. When finally everything worked, there was a real sense of victory! ▶

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AUTHORS

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Bob Fine (page 6) is the Product Line Manager for fixed-point DSP devices. Previously he was Product Support Manager for DSP products and had also managed the DSP Applications Engineering group. Bob initially joined ADI as a designer after obtaining his BSEE from Northeastern University. He has since authored many application notes and technical articles on DSP processors and applications.
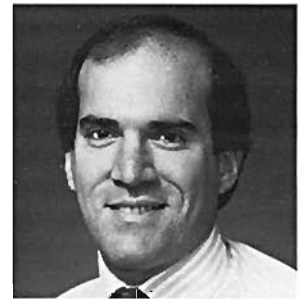
Eamon Nash (page 20) is an Applications Engineer in ADI's Advanced Linear Products group, in Wilmington MA. His photo and a brief biography appeared in *Analog Dialogue* 29-3.

Steve Guinta (page 9) is the Technical Training Manager for ADI's Central Applications Group in Wilmington, MA. His photo and a brief biography appeared in *Analog Dialogue* 29-3.

Cover: The cover illustration was designed and executed by **Shelley Miles**, of *Design Encounters*, Hingham MA.

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Read-Channel Processor Uses PRML to Increase Capacity of MR Head-Based Disk Drives

by Janos Kovacs, Ron Kroesen, Al Haun

The computing world's insatiable appetite for storage capacity continues unabated as new operating systems—such as Windows 95™—applications suites, and multimedia become universally accepted. Typical PC systems are now shipped with hard-disk drives (HDD) capable of storing from 640 MB to 1 GB of information, compared with 340-540 MB in 1994 and 200-300 MB in '93. As the "home PC" has gained acceptance worldwide, HDD unit shipments were pushed to nearly 70 million in 1994 and are expected to exceed 100 million by 1997.

The ongoing challenge for HDD manufacturers is to provide a continuous stream of new products that improve storage capacity at the same (or lower) cost. The principal method of providing a drive that offers both higher capacity and lower cost is to increase storage capacity by increasing *areal density* per platter. Historically, areal density has been improved at the rate of about 30% per year. Recently, however, industry leaders are transitioning to a new trend line improving the rate of increase to over 60% per year.

A variety of techniques and technologies are employed by the HDD designer to meet areal density objectives: improvements in media, head technology, recording modulation, and head-positioning tolerances. This article discusses the key factor of recording modulation technique and how it is matched to the type of head being used in the system. The recording modulation/ demodulation in a disk drive is implemented by the "read-channel processor".

What a read-channel processor is and what it does: The read-channel processor can be looked at as a sophisticated analog-to-digital converter that translates weak analog signals (representing digital information) from a disk drive head to a digital bit stream. In just the past few years the signal processing functions that are included in a read-channel IC have significantly increased in performance and complexity, using *partial-response, maximum-likelihood* (PRML) architecture. PRML bridges the gap between traditional peak-detect pulse extraction and higher performance maximum-likelihood signal-detection schemes employed in communications systems, including modems, digital VCRs, etc.[1]

In a disk drive application the "communication channel" includes:
- A transmitter that transforms binary (0,1) user data into polarity changes of the current in a magnetic coil (*write* head).
- A transmission channel, consisting of a magnetic disk that stores information as changes in the direction of magnetization.
- A receiver that reads the analog signal from the disk and processes it to recover the original binary data.

In today's disk drives, the read-channel processor implements the intelligent transmitter/receiver functions—not including the

[1]See "A high-density recording technology for digital VCRs, by Keiji Kanota et al, 1990 *IEEE Transactions on Consumer Electronics*, volume 36, no. 3.

transducer (write head, write driver electronics) and sensor (read head, read preamplifier) circuitry.

Pulse identification problem: Magnetic transitions on the disk are transformed into voltage pulses with alternating polarity at the output of the read head sensor. An isolated transition in the read channel (which corresponds to a step change in the magnetization) can be approximated by the Lorentzian pulse (Figure 1), given by:

$$l(t) = \frac{1}{1 + \left(\dfrac{2t}{PW50}\right)^2}$$

where PW50 is the time between the points at which the amplitude is 50% of its peak value. The signal peaks as the magnetization changes direction. The data rate at which the user is able to transfer information through the read/write channel can be characterized by the time interval between user bits "T". For a given pulse width, the goal is to pack bits closer, i.e., to increase the PW50/T ratio, which is referred to as *user bit density*.
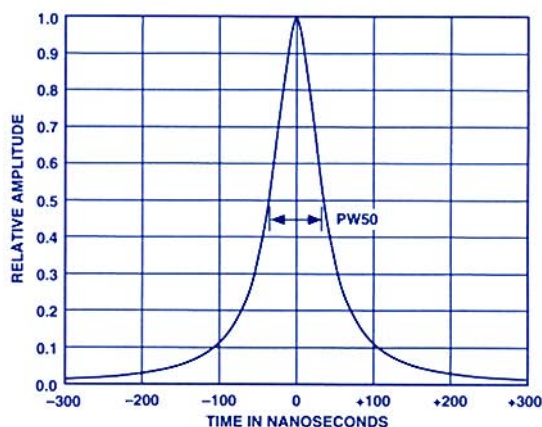

Figure 1. Lorentzian pulse shape, PW50 = 70 ns.

Peak detection vs. PRML: At lower bit densities, where the interaction between adjacent pulses is relatively small, the receiver can be implemented with a peak detector (see *Analog Dialogue* 22-1, 1988). Peaks representing binary "ones" in the read-back signal are detected by operating on the signal with a differentiator, followed by a zero-crossing comparator. The comparator output is gated by an amplitude qualification circuit that disables the digital output pulse when the input read signal amplitude is below a certain threshold value.

A peak detector's operation is continuous in time, and is driven by the input signal only. The industry's first fully integrated "peak-detect" read channel was introduced by Analog Devices with the AD899 family of products.[2] Peak detection is still in use for reading servo information (in head positioning), as a *servo data qualifier* in some present day products.

But as the storage density is increased, the increased interaction between adjacent pulses of opposite polarity produces destructive interference. For a peak detector to operate correctly (i.e., with a low bit error rate) this inter-symbol interference (ISI) and the resulting amplitude decrease and peak shift have to be eliminated. In contrast, *partial response* (PR) signaling (in which each pulse in a neighborhood contributes partially in the process of determining the presence or absence of a pulse in a given location) accepts a controlled amount of interference (cancellation) between neighboring pulses. The most likely (ML = *maximum likelihood*) series of pulses is continually updated, using discrete-time (sampled) signal-processing techniques.

In the various classes and orders of partial-response channels the amount of inter-symbol interference (signal cancellation) is chosen so that only a finite set of discrete amplitudes is generated at the sampling instances when adjacent pulses interfere. In PR4 signalling, which allows the existence of +1, 0, −1 nominal sample values, the isolated pulse is shaped (by continuous and discrete time filters) and the sampling clock phase is adjusted so that only two +1, +1 or −1, −1 sampled values are received; at all other times the samples are zero.

When two magnetic transitions on the disk are at the closest, the corresponding read-back samples (+1, −1) partially cancel, and the resulting sampling of adjacent pulse values is +1, 0, −1. (One could say that each of the transitions is partially responsible for the 0 sample in the middle.) In higher-order partial response systems, like Enhanced PR4 (EPR4), pulse responses due to more than two transitions are allowed to interfere, generating a larger number of possible sample values (e.g., +2, 1, 0, −1, −2, for the EPR4 case).

MR heads: Besides the storage density improvements resulting from the application of sophisticated signal processing techniques, the sta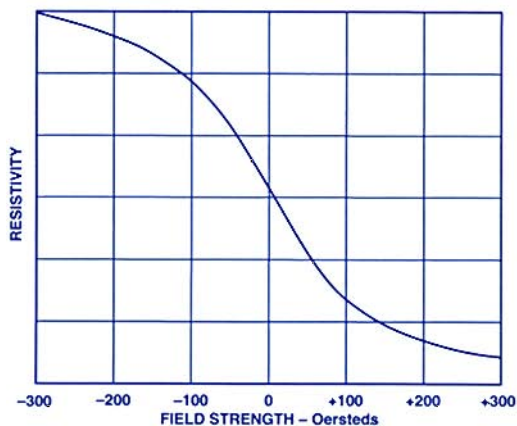ggering rate of increase of disk-drive capacity is largely due to the use of *magnetoresistive* (MR) read heads which are quickly replacing their inductive counterparts. To date, more than 50 million MR heads have been produced, and that number will likely be equalled this year.

MR read heads employ the principle of *anisotropic magnetoresistance* (AMR) to convert magnetic field variations of 5 A/m (oersteds) to about a 2.5% change in resistance. In addition, research continues on GMR (*giant* MR) which yields 5 times the sensitivity of AMR. This allows drive designers to pack more bits into a given surface area, or to relax other design constraints to increase performance elsewhere. [note: even before GMR is implemented in production drives, development of CMR (*colossal* MR) is well under way; CMR holds the promise of very dramatic improvement over GMR.] The sensor itself is a thin film (about 250 Å) of Ni-Fe (nickel iron), also called *permalloy*, and is just a few μm on each side. Modulation in the resistance of the MR element appears as a differential voltage swing at the output of the preamplifier (20-200 mV peak to peak); it is then ac-coupled to the read channel processor inputs (Figure 2).

MR-head asymmetry: MR head technology solves numerous problems associated with inductive heads, such as the dependence of signal amplitude from the platter on its rotational speed. But MR heads have created many new challenges for disk drive designers. One of the problems is the change in resistivity when, occasionally, the MR head touches the disk surface. This contact causes a sudden rise in temperature, resulting in a long-lasting (about 10 μs) voltage transient; to the read channel it appears as a large dc offset with a long tail.

Another issue of concern is the asymmetrical nonlinear transfer function of the MR sensor) due to biasing and the head's off-track position. The asymmetrical read waveform impairs both servo and read channel performance. Furthermore, ac coupling of an asymmetrical signal compounds the problem by introducing dc offset and/or pattern-dependent baseline shift and transients.

Figure 2. MR head response, resistivity vs. field strength.

[2]See *Analog Dialogue* 26-2, pp. 21-22. See also *Conference Record* for 1992 IEEE ISSCC: Kovacs, J. and W. Palmer, "A 32-Mb/s fully integrated Read channel for disk drive applications."

MODELLING COMPLEXITY

To successfully market read-channel chips with the mixed-signal capabilities required for disk drives, time-to-market and design flexibility are of crucial importance. And to enjoy the substantial advantages of "getting it right" the first time, the ability to simulate the entire chip with sufficient accuracy is a big help.

The development of the ADRS120 required great emphasis on enhancing our simulation capabilities. With the cooperation of ADI's CAD department, we developed a highly advanced, proprietary, mixed-signal, mixed-mode simulator, Adice5; it allows: concurrent simulation of analog and digital behavioral models written in C; Verilog code; gate and switch level models; and Spice circuit files. Precision and extremely fast execution is guaranteed by fully integrating a Spice-like circuit simulation engine with an event-driven timing simulator environment.

We invested significant engineering time in behavioral model development and optimization of all-analog circuitry to enable chip-level simulation of all functions of the read-channel processor. This simulation environment facilitates the use of large sections of the chip as a "software prototyping board", where behavioral models of the surrounding blocks provide realistic stimulus to a smaller circuit simulated at the transistor level.

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By considering MR head-related problems in the design of the read-channel chip, semiconductor vendors like Analog Devices can add significant value to the disk-drive electronics. This is exemplified in the ADRS1xx family.

Product features: Parts in the ADRS1xx family are available with a variety of signal-processing functions and options. They offer a complete signal-processing solution for state-of-the-art disk drives, especially when MR technology is combined with PRML processing. The circuit blocks are implemented in CMOS, which permits timely delivery of cost-effective semicustom chips.

Figure 3 is a block diagram of a typical ADRS1xx read-channel chip. An assortment of continuous and discrete time filters realize the necessary combination of low-pass noise filtering and frequency boost for pulse slimming. A 7th order equiripple filter with two independently programmable zeros, in combination with an analog *or* digital 5-tap, adaptive FIR filter, carries out low-pass filtering and equalization of the read-back signal to a PR4 target. The option of shaping the analog signal in the sampled analog domain, before the quantization process takes place, can eliminate the enhancement of quantization noise and reduces the effective number of bits (ENOB) required in the A/D converter.

A patented dual analog/digital automatic gain control (AGC) loop in tandem with a hybrid phase locked loop (H-PLL) take care of adjusting both the amplitude and the sampling instance of the read signal. Gain switching during acquisition and tracking with programmable damping factor in the PLL assures easy optimization of the loop dynamics. In addition, the use of active offset cancellation in the analog front end, together with a user-activated clamping function (time constant reduction of the AC coupling networks), can significantly shorten the recovery time from offset transients (thermal asperity).

A/D Converter: The ADC is a full-flash type, 6-bit, 144-MSPS (megasamples per second), with built-in patented MR head asymmetry correction. The MR head asymmetry is eliminated using the ADC's gain correction and/or dc offset correction; each ADRS1xx provides registers to store user-programmed correction code. In larger disk drives with multiple platters—and multiple MR heads—correction code for each platter is stored on the drive for on-the-fly switching.

PR4 and EPR4 Viterbi detectors implement *maximum likelihood* detection (PRML). Unlike peak detectors that make consecutive irrevocable decisions, bit by bit, as to whether a peak was greater than a certain fixed threshold, maximum likelihood detectors compare sequences of signal samples to all possible combinations and pick the one that matches the received signal sequence the best. Viterbi detectors perform maximum likelihood detection in a recursive fashion, i.e., by executing some of the computation at every "bit time". A set of threshold values are dynamically adjusted, based on previous signal samples, and compared to the latest signal sample (US patent 5,373,400).

Each of these tentative (soft) decisions can and will be modified at a later time (within limits of the available memory) if additional signal samples indicate that a previous decision was wrong.

Evaluation board with Windows Software: Lab experiments and characterization of the part are simplified by the availability of an evaluation kit. The kit includes National Instruments' LabView®-based software for evaluating the ADRS120 with either a spin stand or on a stand-alone basis. The evaluation board plugs into the parallel port of a 486 (or Pentium class) PC running Windows™. The board provides all the components necessary to operate any member of the ADRS1xx family (Figure 4).

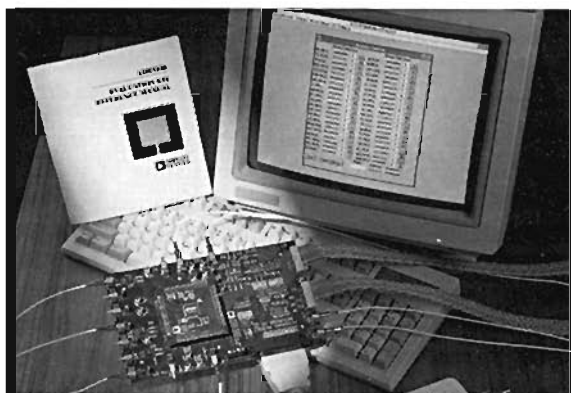The ADRS120 is available in an 80-lead PQFP
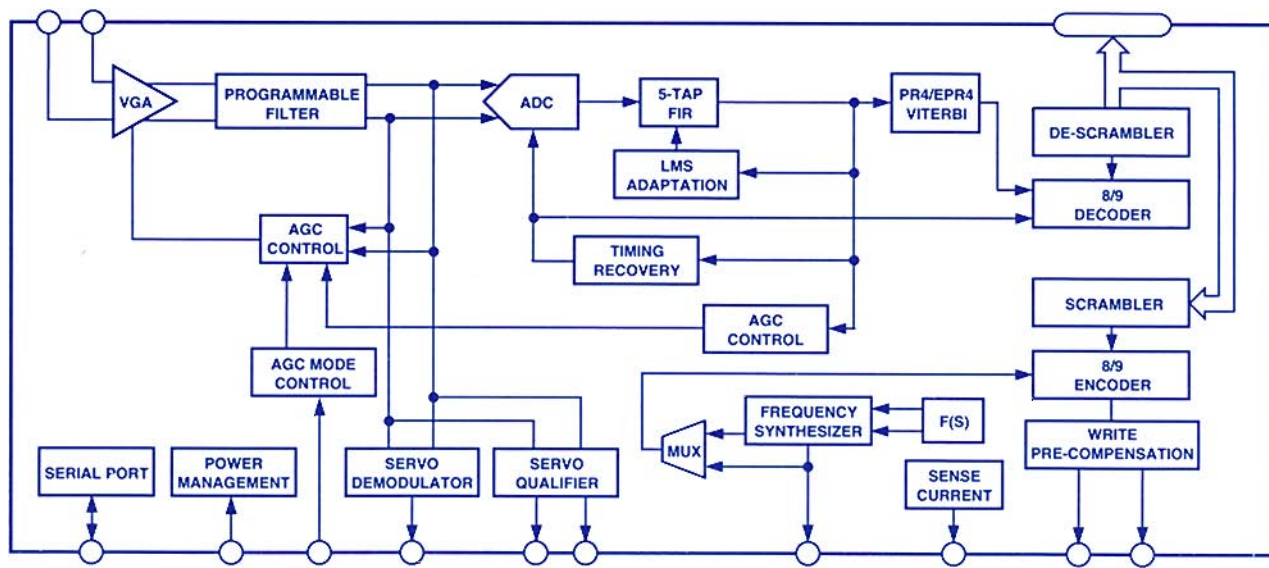
Figure 4. Photograph of evaluation kit.

Figure 3. Block diagram of integrated read channel.

New Fixed-Point DSP Family Provides High-Performance Processing of Concurrent Signals

Architectural innovations in new DSP core processing unit improves the efficiency of high-level language implementations

by Bob Fine

The ADSP-21csp01* is the first member of a new Analog Devices family of 16-bit fixed-point digital signal processors designed specifically for rapid and efficient processing of multiple signals concurrently—and to efficiently process compiled code written in a high-level language. Its core design permits more software to be written and debugged in C, simplifying development of fixed-point DSP applications and speeding time-to-market for product and system designers. Applications such as simultaneous voice-over-data modems, cellular basestations, and computer telephony systems benefit from improved DSP throughput, reduced chip count, and faster time-to-market.

Its newly designed architecture (Figure 1) comprises an arithmetic section supported by a large set of general purpose data registers; a data-address generation section consisting of two address generators; and a program sequencer supported by a 64-word instruction cache. This core is augmented by an ample 20 kilobytes of on-chip SRAM, configured as 4 K × 24 program memory RAM and 4 K × 16 data memory RAM, a 16-bit DMA (direct memory-access) port, two serial ports with DMA and a boot controller. These features—combined with the 50-MIPS (million instructions per second) performance of the ADSP-21csp01 and the 24-bit address bus—supply the processing horsepower and I/O bandwidth required for processing multiple signals concurrently.
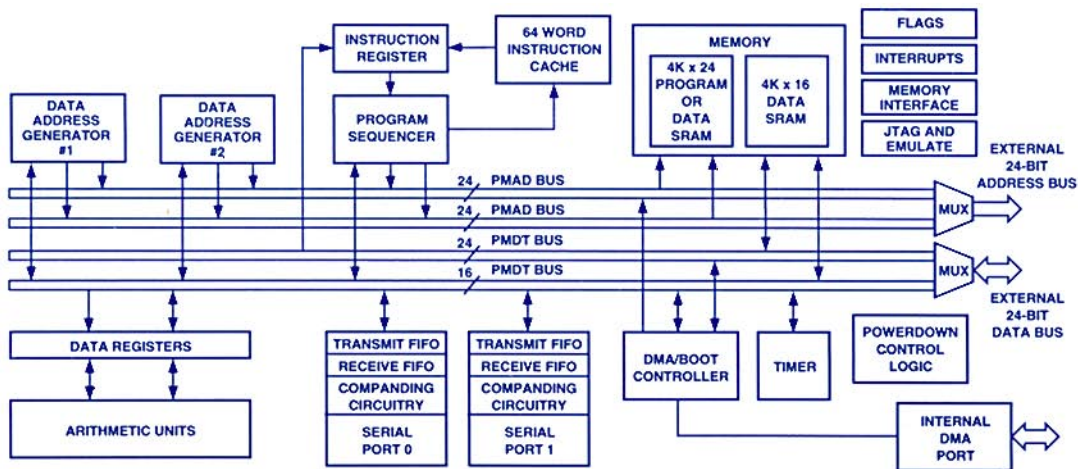
CONCURRENT SIGNAL PROCESSING

Inexorable trends are driving signal-processing systems to smaller size, lower cost, lower power consumption and higher performance—and they are significantly influencing the direction of DSP architecture. The new high-performance processors must be designed with the capability to perform tasks that previously would have required several processors (Figure 2).
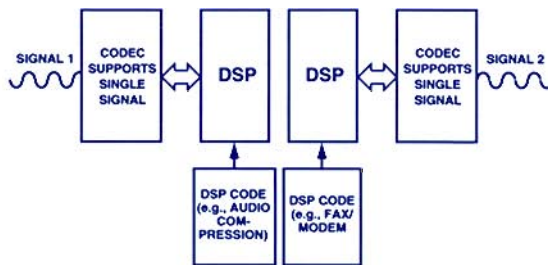
Figure 2. System Requiring two processors.

More importantly, emerging applications, such as voice-over-data modems—which simultaneously process modem/FAX signals as well as speech signals—impose requirements on the DSP to process concurrent signals.

To accomplish this, the DSP must be able to address a large program- and data memory space—large enough to store the program instructions and data for all the algorithms required by the application. The DSP must also have enough speed and efficiency to execute the multiple algorithms and perform the multiple tasks of the application in real time. Furthermore, to accommodate the multiple signals used in the application, the DSP must also have multiple I/O ports, plus DMA channels to stream data in and out of the DSP's internal memory without interrupting the processor (Figure 3).

Figure 3. System employing a single DSP.

Figure 1. ADSP-21csp01 internal architecture

*For technical data, use our web site http://www.analog.com

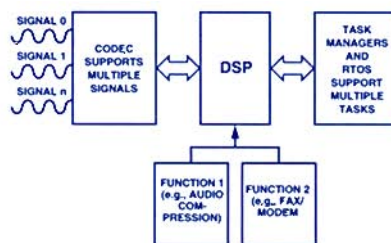A powerful solution is the ADSP-21csp01 Concurrent Signal Processor. With its 50-MIPS instruction rate, highly paralleled instruction set to perform many operations in a single cycle (550 MOPS), 24-bit address reach to access up to 16 Mwords of instructions and data, high I/O bandwidth and DMA channels—it can accommodate the multiple signals from a codec (or multiple codecs) and can handle multiple tasks in real time.

ARCHITECTURAL DETAILS

The arithmetic section of the ADSP-21csp01 consists of a 16-bit arithmetic/logic unit (ALU) and a 16×16-bit multiplier/accumulator (MAC), with dual 40-bit accumulators, and a barrel shifter. The single-cycle, non-pipelined arithmetic units operate independently of one another and have provisions for multi-precision operations. The 21csp core has a total of 96 on-chip registers, including 64 addressing registers and 32 arithmetic registers, including two sets of multiply result-registers. Two banks of data registers provide data operands to the arithmetic units and store arithmetic results. Any data register(s) can be used to supply a data operand to any arithmetic unit. This high degree of flexibility simplifies programming and enhances the efficiency of systems implemented with high-level languages. The arrangement of data registers in a primary bank and secondary bank simplifies task switching, since it takes only a single cycle to switch between register banks.

The address generators of the ADSP-21csp01 allow data to be accessed with indirect addressing using an *address* (I) register in conjunction with a *modify* (M) register or an immediate modify value. 16 sets of these registers are arranged in a primary bank and a secondary bank. Updating of the address can be performed in both a pre- and post-update mode (i.e., before and after the address is outputted to the address bus). Zero-overhead looping instructions that can nest up to five levels produce fast, efficient, and tightly coded loops.

To support the automatic maintenance of circular buffers (with an absolute minimum of instructions), the address generators also employ a set of *length* (L) registers and *base* (B) registers. As many as 16 circular buffers can be maintained (8 with the primary registers and another 8 with the secondary registers)—with a starting address for each at any memory location. The ability to maintain many circular buffers simultaneously is a key advantage in the processing of multiple signals concurrently, since the data set associated with each signal needs to reside in its own buffer. Also, an algorithm that processes a single signal might require several circular buffers. This requirement gets multiplied when concurrent signals are to be processed. With address generators dedicated to each circular buffer, no extra processing time is required to swap pointer values in and out of address registers.

The program sequencer is used in conjunction with a 64-word instruction cache to sustain three-bus performance for fetching

an instruction and two data values. The cache is selective: only the instructions whose fetches conflict with program memory data accesses are cached. This allows full-speed execution of core, looped operations such as digital filter multiply-accumulates and processing of FFT butterflies.

Another important aspect of efficiently processing multiple signals in real time is *interrupt latency*. The ADSP-21csp01 responds to external and internal interrupts in a minimal amount of time. This is an extremely important factor, since response time to the external signals is critical to real-time performance.

UNIFIED MEMORY SPACE

Modified Harvard architecture, a key characteristic of a DSP, allows two data words, as well as the next instruction, to be fetched in a single cycle. This three-bus performance is what sets a DSP apart from other microprocessors and RISC processors. Traditionally, DSP memories have been configured into two separate spaces to support the Harvard architecture. These two memory sections offer the efficiency required in the dual operand fetch, but at the cost of flexibility. For example, the DSP might have a total of 8 K words of memory arranged as two separate 4-K word blocks. However, the particular application might have a need for a total of 8 K words—deployed as a 6-K-word program section and a 2-K-word data section. The DSP's memory space has enough total memory, but not in the needed configuration. The result is a need for external memory to make up the difference.

The ADSP-21csp01 eliminates this problem by providing memory in a unified undedicated address space. This memory is *multiported* to accommodate the fetch of two data operands in a single cycle—with optimal flexibility. Any portion of the memory can be used for program instructions or for data stored in either program memory or data memory.

This memory configuration also provides additional flexibility required by a high-level language, such as a C compiler.

DEVELOPMENT TOOLS

The architectural innovations of the ADSP-21csp01 are accompanied by new advances in development tools. An integrated development environment (IDE) running under Windows 95 allows the definition of a project where assembly, linking and project building are performed in a single step. An environment menu lets the user specify assembler and linker options to eliminate the older command line use of switches. The IDE remembers user preferences and settings, as well as all the names of files comprising the project. After the initial IDE set-up, code generation and debug can be performed quickly.

The ADSP-21csp01 EZ-ICE (In-Circuit Emulator, with its easy-to-use Microsoft Windows interface) allows non-intrusive access to the internal processor registers through a JTAG serial boundary-scan interface. Consisting of a PC plug-in card and a small attached probe, the EZ-ICE supports full-speed operation, up to 30 software breakpoints, nine hardware break ranges, single-step execution, register Modify and Read, and program and data memory upload/download.

The ADSP-21csp01 EZ-LAB is a PC plug-in development system that includes an ADSP-21csp01 with a connector for analog front end cards. The EZ-LAB board can also be operated in stand-alone mode, booting from the on-board EPROM. Software is included for program debugging.
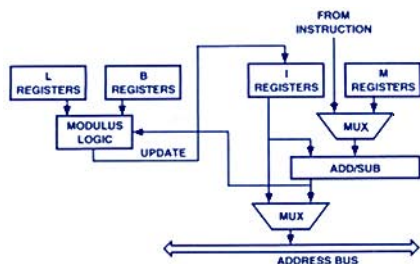

Figure 4. Address-generator architecture.

HIGH-LEVEL-LANGUAGE PROGRAMMING

As demands are placed on system manufacturers to get products to market quicker, designers are required to employ methods that keep the design cycle as short as possible. Also, algorithms and standards are changing at an increasing rate. Development methods that can simplify the creation of code and preserve existing code by making it more transportable among different platforms offer key benefits to system designers. High-level languages, such as ANSI C, can provide this level of simplified code generation and transportability for the large and growing number of skilled C programmers..

The ADSP-21csp01 features a new DSP core, which includes key architectural features for efficient implementation of C compilers. The program sequencer supports PC-relative jumps and calls. PC-relative capability simplifies relocatable code. The large number of registers and the flexibility to use a single register to store a variable used in different arithmetic operations improves the computational efficiency and ensures optimum data flow of compiled code. The C compiler does not need to generate additional instructions in order to save and restore values to and from the registers. The address generator architecture provides the functions required for efficient stack maintenance. The C compiler can manipulate frame pointers and generate linked lists with significantly fewer instructions.

Overall, the architectural features of the ADSP-21csp01 allow for a C compiler that generates code three to five times more efficiently than the earlier Analog Devices ADSP-21xx family.

The ADSP-21csp01 is housed in a 160-lead PQFP package and will be in production in mid 1996. Samples, and the beta version of the development tools, will be available in late spring. ▶

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DSP ARCHITECTURE STREAMLINES HIGH-LEVEL-LANGUAGE PERFORMANCE

Traditionally, software developed for fixed-point digital signal processors (DSPs) has been written in assembly code to meet system performance and system cost needs. However, as DSP performance increases and cost decreases, designers are expanding its role to include system processing functions, in addition to signal processing. As a result, DSP code size is increasing, and software development time is skyrocketing. New methodologies for DSP software development are long overdue.

Coding dilemma: In developing code for DSP-based systems, software engineers often struggle to write programs that are both efficient and transportable, balancing the benefits and drawbacks of low- and high-level programming. Low-level assembly-language programming yields tightly written, efficient code. However, it requires processor-specific expertise and is more exacting to use than higher-level language. As programs grow in size and complexity, the job of assembly language programming becomes increasingly daunting. And the design effort tends to be wasted, because assembly code is troublesome to transport to other system applications.

To boost their productivity, software engineers prefer to write in the popular ANSI (American National Standards Institute) C, with its rich library of functions. Machine-independent, it is transportable—but it tends to be inefficient. Inefficient code diminishes a DSPs capacity for real-time signal processing and increases system cost by requiring more memory for storing programs and data.

Good compiler design can improve C's efficiency somewhat. But what really hurts is that, for transportable code, assumptions must be made about the program's overall function and the DSP's internal hardware. Inadequate hardware design can lead to a much higher code overhead. Thus, some of the advances embodied in the csp01 family, besides providing improved hardware performance, also permit more-efficient high-level software to be written. In particular, improvements in the way the stack is handled, how memory is used, how data flows, and how computations are done—the areas most affected in C programs for DSP—are resulting in more-efficient execution.

Spill resistant: Efficient use of DSP registers is one way a C compiler can streamline code. For example, a compiler that minimizes data swapping into and out of registers, especially for storing temporary data or intermediate results, will produce cleaner code than one that doesn't. To this end, the DSP's architecture helps by allowing registers to hold input values for all arithmetic operations. In addition, with an ample supply of registers, the chip minimizes register storage conflicts, or *spills*, further raising efficiency and speeding the flow of data.

Consider how a DSP's register-set can avoid conflicts and help a compiler translate high-level language into tight code. Register spills can add power-robbing program statements; they occur when one register storing valid data is called upon to load a new value. If all available registers contain needed data, the contents of one register must be temporarily moved to make room for the new data word. The resulting spill requires the compiler to add instructions that execute and then restore the temporary data swap. These instructions become overhead that cuts a program's efficiency.

An example might occur in a voice or audio mixing application. Several channels are to be scaled (volume adjusted), then mixed together. In this case, a unique multiplier factor (gain) is used for each channel. In most DSPs the gain (or *volume variable*) for each channel would have to be loaded from memory or an external register each time it is used. The multiplicity of registers in the csp01 permits each variable to be loaded into one of 16 registers, where it is immediately available when needed.

Again, the ADSP-21csp01 has two dedicated registers for storing multiplication results. Thus, two sets of results (say, filter parameters) can share the same multiplier output. Beyond this, any of the three functional units within the arithmetic section (multiplier, ALU, barrel shifter) can store input data in *any* of the arithmetic registers. In contrast, DSP architectures that traditionally dedicate specific registers for holding input values are more inclined to cause spills.

The use of registers is just one example of code savings. Other contributors are the lean code for maintaining the DSP's stack and accessing data arrays and structures using linked lists, fitting C compilers like a glove. Indirect addressing saves code and time in subroutines. And of course, the multiple use of buses for data in the device's Harvard architecture permits simultaneous data fetches from a common memory space. All of this adds up to strong encouragement to the designer to write more of the design cycle in C, thus lowering the DSP software development barrier and restoring time-to-market goals.

Considerations In Designing Single Supply, Low-Power Systems Part II: Battery Powered Systems

by Steve Guinta

Part I of this two-part series (Designs using ac line power) appeared in the last issue of Analog Dialogue (29-3). In it, we discussed the implications and performance tradeoffs in converting to a single-supply system using conventional (i.e., non-single supply characterized) active devices, such as op amps, A/D and D/A converters, etc., then further described several new product families and processes from Analog Devices that provided single-supply operation without the limitations on speed and dynamic range of conventional devices. We continue here with the considerations involved in design for low-power operation, particularly for portable and remote applications with batteries.

BATTERY-POWERED SYSTEMS

In a battery-powered system, *time* is the critical parameter. Unlike ac-powered systems, where supply voltage varies within a specified range and the availability of rated current is unlimited in duration, a battery can only supply power for a finite length of time before it requires recharging or replacement. In addition, as the battery discharges, the greater the current drain, the greater the drop in battery voltage (or *supply rail*) (Figure 1).
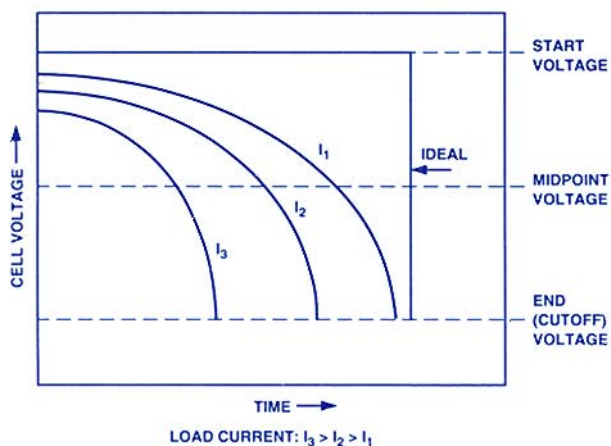

Figure 1. Cell discharge as a function of current discharge rate.]

The key to designing an efficient battery-operated system, then, is (a) to maximize battery life by minimizing the current drawn by the circuit, especially the continuous "quiescent current"; and (b) if necessary, to maintain the voltage supplied to the load at a constant level during discharge by using some form of regulating circuit between the battery and the load. For example, a battery with a capacity of 100 mA-hour powering a circuit that draws 1 mA will operate for approximately 100 hours before recharging or

replacement is required. If this quiescent current is reduced to 100 µA, the battery life ideally increases to about 1,000 hours.

Before designing a battery-operated system, it is important to understand the environment, requirements, and operating conditions under which the system will be used; this will allow the designer to determine what type of battery should be used (for example, primary or secondary), and how often the batteries would need to be replaced or recharged.

For example, systems such as portable industrial data loggers or emergency medical monitors often can be recharged overnight (or when not in use), and so a *secondary*, or rechargeable, battery could be used. On the other hand, such low-power, battery-powered equipment as remote weather stations, seismic data recorders, or signalling beacons might be required to operate for weeks or even months without battery replacement or recharging; for such applications, a "throwaway" primary-type battery might be chosen.

Regulating the battery output: A regulator between the battery and the load keeps the supply rail at constant voltage during battery discharge. This can be important for several reasons:

• With operational amplifiers and other similar linear devices, changes in power-supply voltage can unbalance the dc input offset voltage from its pre-trimmed value. In most cases, this slight change in offset might have little or no effect on the accuracy of the system; however, in high-accuracy or low-level applications this could be a problem.

For example, most precision op amps exhibit a power supply rejection (PSR) at DC of the order of 120 to 100 dB. This is equivalent to 1 to 10 microvolts per volt of supply change. If the supply (battery) voltage were to drop from 5.0 V to 3.0 V, then the shift in input offset voltage would be

$$\Delta E_{OS} = \frac{\Delta Vsupply}{PSRR}$$

For a supply rejection of 100 dB (to 0.001%), this would equate to an offset change of 20 µV. This could represent a substantial number of degrees in a temperature monitoring system using sensitive B, R, and S type thermocouples, with temperature sensitivities of the order of 10 µV/°C or less.
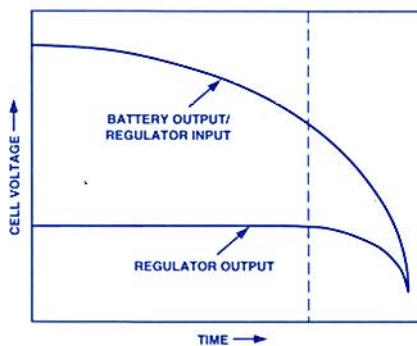

Figure 2. Voltage regulator and effect of battery discharge.

• Some designers may use the supply rail as the reference for analog-to-digital and/or digital-to-analog converters. Unless the measurement is ratiometric, the use of raw battery output as a voltage reference can lead to accuracy problems. For example, a two-volt shift in battery voltage can cause a 40% drop in the scale factor of a data converter. An n-bit A/D or D/A converter has an LSB (least-significant bit) weight of $V_{REF}/2^n$. Comparing 5 V with 3 V of supply voltage, used as a reference:

2^n	5 V	3	V
2^{-12}	1.22 mV	732	μV
2^{-16}	76 μV	46	μV

Voltage regulator devices, such as the REF19x series, are useful in stabilizing supply or reference voltage. They will maintain their output voltage at a constant level until the regulator reaches its "drop-out" voltage, i.e., the value at which the regulator can no longer hold its output constant (Figure 2).

The use of a regulator does require somewhat higher battery voltage, but a type with low dropout voltage can minimize the use of additional cells. For example, the 3-V REF193's dropout voltage ranges from 0.8 V with 10-mA load to 0.3 V with minimal load.

Extending Battery Life: Three ways to extend battery operation are: (1) Minimize the quiescent current if continuous operation is needed; (2) Pulse the load on and off so that the battery operates on a lower duty cycle; and (3) Power down the circuit when not in use.
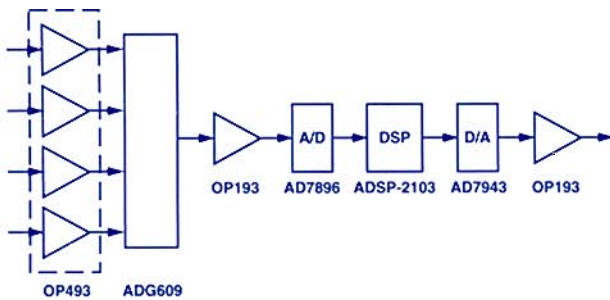
(1) Minimizing quiescent current: The overall quiescent current in the system can be minimized by

(a) proportionately increasing the values of all the bias resistors in the circuit (not always a good idea, since it can lead to higher levels of Johnson or resistor noise)

(b) using monolithic devices, such as op amps or data converters that have been designed to operate from a single +3-V to +5-V supply rail at low power (<1 mA) or "micropower" (<100 μA) levels. The choice of solutions is expanding as more devices become available on the market, to meet a variety of operating power budgets; included are: op amps, data converters, multiplexers, switches, references, etc.

Figure 3 is an example of a typical, battery-operated, multi-channel data acquisition "signal chain" using single-supply, low-power devices.

(2) Pulsing the load on and off: This is a useful approach when sampled measurements are required. The REF19x series, for example, have a TTL "sleep" control input, which permits a load drawing, say 15 mA, to be periodically switched on and off, with a residual quiescent current drain of 5 μA.

(3) Powering Down The Circuit: Powering down the circuitry (the general case of pulsing the load on and off) is another way to conserve battery power. Like the pulsed case, it has some potential problems that need to be understood before it is implemented:

(a) Time must be allowed for all circuitry to settle out after the battery is turned on. A salient example is the internal (or external) voltage reference used for A/D and/or D/A converters. If sufficient time is not allowed after turn-on for the reference to stabilize, and an A-D conversion or D-A update is performed, a gain error will occur. The settling time required is further increased if the reference output is filtered to reduce noise; the filter capacitance will require additional time to charge up to its full value.

(b) It is not a good idea to power down an amplifier or data converter while an analog or digital signal is still applied. In the case of an op amp, applying a positive signal to an unprotected op amp's positive or negative input with no power to the supply rail causes a forward biasing of an internal p-n junction that causes current to flow from the signal source to the supply rail (Figure 4). If current is allowed to flow in an unprotected amplifier over a sufficient period of time, damage can occur to the amplifier due to "metal migration" or degradation (evaporation) of the trace.
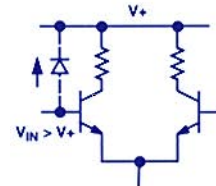
Figure 4. Forward-biased internal P-N junction.

The same problem exists for A-D and D-A converters, if the power supply is turned off, but input logic signals are still active at the converter's digital inputs.

PART NO.	DESCRIPTION	SUPPLY CURRENT
OP193	OP AMP	22μA
OP493	OP AMP	88μA
ADG609	CMOS MUX	2μA
AD7896	A/D CONVERTER	4mA
AD7943	D/A CONVERTER	5μA
ADSP-2103	DSP	20mA

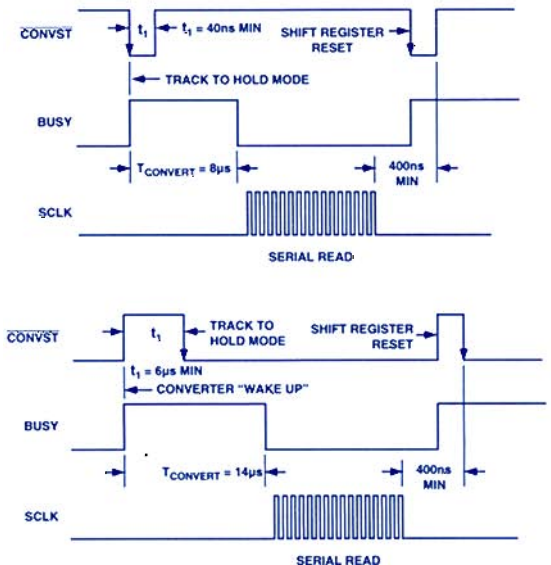Figure 3. A complete, 3-V-powered data acquisition system.

Figure 5. Timing diagrams for the AD7896, showing normal mode of operation (a) vs. sleep mode (b).

(c) Many of the newer, low power devices available on the market today feature a power-down or "sleep" mode of operation, where certain functions of the device are shut down to conserve power, but the device itself is still "active" in that it retains its operating state. For example, a D/A converter that is powered down will still retain its latched digital data. Devices that feature power-down or "sleep" mode of operation generally are designed not to be affected by analog or digital signals present at their inputs during power down mode.

An example of a device that offers a unique feature is the AD7896 12-Bit Sampling A/D Converter. The AD7896 features a proprietary, automatic power down mode, in which the A/D automatically goes into a "sleep" mode once conversion is complete, and "wakes up" automatically before the next conversion cycle. During the "sleep" mode of operation, quiescent current is reduced thousandfold, from 4 mA to 5 µA. ▶

A PRIMER ON BATTERIES

A *battery* consists of an energy cell or a group of cells stacked in series for higher voltage or in parallel for higher output current.
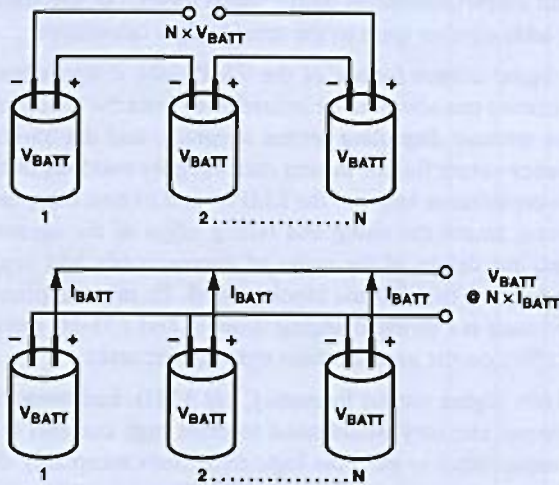
The electrical energy of a battery cell is produced by a chemical reaction between its anode, cathode and electrolyte materials. It is worth noting that, in battery terminology, the positive terminal is the *cathode*, the negative terminal is the *anode*.
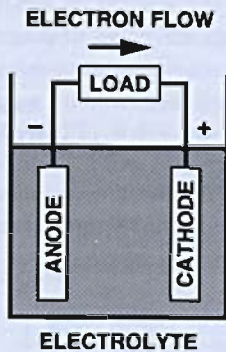
The materials used for the anode, cathode and electrolyte and their quantity, primarily determine the battery's output capacity, specified in ampere-hours (Ah) or watt-hours, (Wh). Other factors, such as energy density (Ah/kg), relative size, cost, thermal stability, storage life, etc., are also a function of the choice of materials. The illustration compares discharge characteristics for several primary battery types. [from *The Art of Electronics*, 2nd edition, by Paul Horowitz and Winfield Hill, as adapted by the authors from battery literature. Cambridge (UK): Cambridge University Press, 1989.]
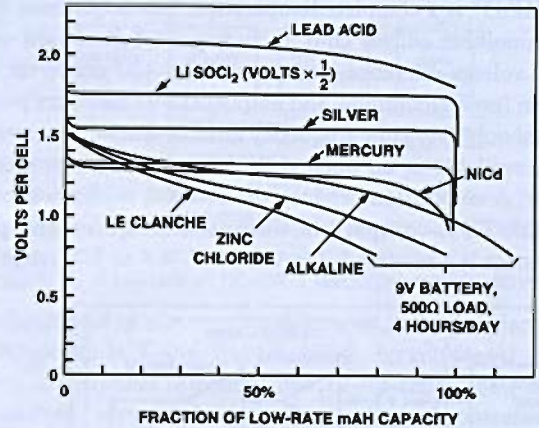
Batteries are classified as either primary (non-rechargeable), secondary (rechargable) or reserve (inactive until activated):

a) Primary batteries are often relatively inexpensive; they are usually found in applications where long-term operation with minimal current drain is expected. Examples include a car's miniature, remote activation device for "keyless" entry/alarm, portable hand-held multimeters, portable remote data-loggers, remote or emergency signalling devices, etc. The standard AA, C and D-size dry-cell batteries found in radios, flashlights, toys, etc., are examples of low-cost, consumer-type primary batteries.

b) Secondary batteries have the advantage of being rechargeable; they are often found in applications such as the battery backup in an ac-powered system, (e.g., mainframe computers or emergency lighting systems) where the secondary battery is continuously charged by the system, or in applications where bursts of high-energy output for short periods of time are required, such as in portable power tools.

c) Reserve batteries are designed for very long term storage, and cannot provide any output until a key chemical element (usually the electrolyte) is added. A car's 12 volt battery on the automotive dealer's shelf is an example of a reserve battery.

The following chart lists the most commonly known battery types, and their properties:

Battery	Type	Anode	Cathode	Cell Volts	Ah/kg
Alkaline	Primary	Zn	MNO_2	1.5	224
Lithium	Primary	Li	MNO_2	3.5	286
Lithium	Primary	Li	SO_2	3.1	379
Lead-acid	Secondary	Pb	PbO_2	2.1	120
Nickel-Cad'mium (Ni-Cd)	Secondary	Cd	Ni Oxide	1.35	181
Nickel Metal-Hydride	Secondary	MH	Ni Oxide	1.35	206

Source: Handbook of Batteries, 2nd edition, by David Linden. New York: McGraw-Hill, 1995.

Digital-Output Sensor Simplifies Temperature Acquisition

by Andy Jenkins (Analog Devices) and
Jeff Lewis, (Display Graphics, San Diego)

The TMP03* is a complete temperature data-acquisition system on a monolithic silicon chip. Including a silicon-based sensor, internal voltage reference, and sigma-delta A/D converter, it fits in a 3-pin (power, common, and output) TO-92 transistor package. Its digital output is a low-frequency variable-duty-cycle serial data stream, available at an open collector with 5-mA sink-current available. A companion product, the TMP04, is identical but has a CMOS/TTL-compatible output. The quiescent power requirement is a modest 1.3 mA at +5 V (4.5 to 7-V range).
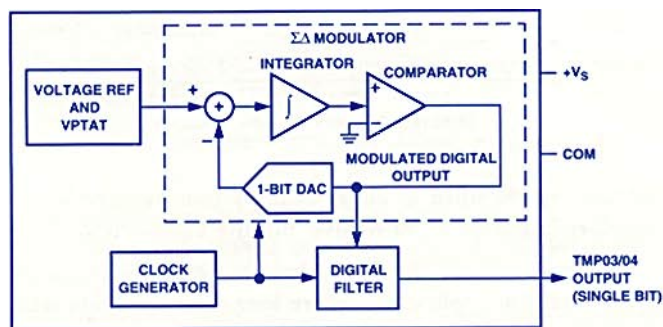

Figure 1. Functional block diagram of the TMP03/TMP04, with its sigma-delta modulator.

Integrating the whole temperature-to-digital chain on a single chip saves space, design time, and money. In addition, the digital output and small number of leads enhances reliability and greatly simplifies isolation and remote operation. With fewer error sources, computation of the error budget is easier. The TMP03's digital output allows multi-channel systems to be constructed easily (additional sensors share a single-channel low-cost digitally-multiplexed decoder). Our TMP03 Evaluation Board is an example of low-cost multi-channel temperature-acquisition.

Typical applications of the TMP03 exist "everywhere"; a few examples include isolated sensors, environmental control systems, computer thermal monitoring, thermal protection, industrial process control, and power-system monitors.

Device Description: Analog Devices bandgap references generate both a constant voltage and a PTAT (proportional to absolute temperature) voltage. In the TMP03, these are applied as inputs to a first-order sigma-delta modulator. The device output is a 35-Hz (nominal) accurately mark-space-modulated digital signal that is insensitive to frequency. The TTL/CMOS compatible output allows the TMP03 to interface directly to standard logic.

Thus the TMP03 and TMP04 are well suited to interface directly to a microcontroller timer/counter input port and programmable logic arrays. The TMP04 provides a high-output-current logic output capable of driving a load capacitance of 1000 pF with minimal loss of switching-edge definition.

System Specifications: Since it is completely self-contained, the TMP03/TMP04 has specifications that are close to the final system specifications. A single temperature accuracy specification for the TMP03/04 combines errors due to the sensor's transfer function, signal conditioning and conversion. Typical accuracy (–25 to +100°C) is to within 1.5% (4% max), with nonlinearity of 0.5°C and power supply sensitivity of 0.7°C/V (1.2°C/V max). The device's operating temperature range is –55°C to +150°C.

Remote Operation: Outputs of traditional low-level voltage-output temperature transducers, when located remotely, will inevitably suffer signal degradation and errors due to noise pickup and/or ohmic losses. Some sensor schemes rely on analog output conditioning to produce a current output for long distance transmission (e.g., conventional 4-20 mA current loop). The current output eliminates ohmic signal losses, but the additional stage adds another term to the error budget calculation.

The digital output format of the TMP03/04 design allows this temperature transducer to be located away from the host computer system without degrading system accuracy; and the 35-Hz low-frequency output further insures data integrity over long distances. Cable capacitance between the TMP03 and its host computer will of course round the rising and falling edges of the square-wave output, but delays of the order of microseconds add negligible error relative to a 29-ms clock period. In most applications, temperature is a slowly changing variable, and a 35-Hz carrier has little effect on the measurement dynamic accuracy.

If a 100× higher output frequency, say 3 kHz, had been chosen, the output circuitry would need to drive high currents into the load capacitance to keep the logic transitions acceptably short; a 1-μs asymmetry between the rise and fall times would have added about 1°C error. High output current requirements also increase the required supply current. An alternative solution for high-frequency, low-level transducer output: i.e., adding a local RS-232 (or RS-485) interface to drive a long cable, again increases the remotely supplied current required.

The table compares the sources of errors in a TMP03 based temperature measurement system to those in a system based on conventional analog temperature transducers:

	Thermocouple, Thermistor, RTD, etc.	TMP03
Sensor Error:		
Nonlinearity, hysteresis, long-term drift	X	X
Signal Conditioning:		
Nonlinearity, cold junction compensation drift, hysteresis, gain drift, offset (over temp range)	X	NA
Digitization:		
Nonlinearity, hysteresis, drift, missing codes, offset, charge transfer, reference drift	X	X
Reference:		
Drift with temp; drift over time	X	NA
Signal degradation over distance	X	NA
Multiplexer errors (multi channel systems)	X	NA

Only two terms are necessary for error budget calculation in the TMP03—the data sheet temperature measurement error spec and the quantization error for the external digital decode circuitry. A spreadsheet calculation can be used to select the desired counter resolution for the external digital decode circuitry. A 12-bit digital counter decode scheme introduces only 0.5°F quantization error.

TMP03 Output Decoding: The TMP03 sensor uses mark-space ratio modulation (Figure 2), embodying the relationships

$$Temp_{\circ C} = 235 - \frac{T_H}{T_L} \times 400$$

$$Temp_{\circ F} = 455 - \frac{T_H}{T_L} \times 720 \qquad \text{(Eq. 1)}$$

where T_H and T_L are the high and low periods of the square-wave output.
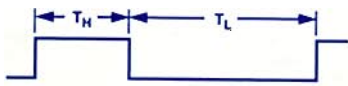

Figure 2. Mark-space ratio modulated square-wave output.

With the basic TMP03 sensor error specs, errors introduced in measuring T_H and T_L are the only other parameters needed to determine system accuracy. For example, if T_H and T_L are measured using a 125-kHz clock frequency and 12-bit counters, gated by the edges of the square-wave output, the quantization error is less than 0.5°F. T_H and T_L may be conveniently measured using discrete counters, programmable logic arrays, or from a microprocessor with an on-board timer/counter port. If absolute temperature is required, it can be calculated using a microprocessor or PC. The table indicates typical counter resolutions used in establishing T_H and T_L values, and the associated bit-error values at the various clock rates. The method of calculation is described in the TMP03/TMP04 data sheet.

Table 1. Counter Size and Clock Frequency Effects on Quantization Error

Maximum Count Available	Maximum Temp. Reqd.	Maximum Frequency	Quantization Error (25°C)	Quantization Error (77°F)
4096	125°C	94 kHz	0.284°C	0.512°F
8192	125°C	188 kHz	0.142°C	0.256°F
16384	125°C	376 kHz	0.071°C	0.128°F

A frequency of 125 kHz is used in the evaluation board; it allows temperature measurement to 85°C (plus ~10°C over-range) and provides approximately 0.3°C resolution.

TMP03 Design Example—the Evaluation Board: A temperature measurement system was constructed using a programmable logic device for input multiplexing (of the TMP03 signals) and to derive T_H and T_L, a 5-V RS-232 converter, and a connector for up to eight TMP03s (Figure 3). This 8-channel temperature measurement system connects to the serial port of a IBM-compatible personal computer and allows temperature data to be gathered and recorded from remotely mounted TMP03 sensors. The PC selects the temperature sensor, logs data and performs the temperature calculation.

The PC first transmits the channel select byte. The digitally encoded temperature information from the TMP03 (the T_H/T_L square wave) is decoded using the programmable logic device, and the T_H and T_L count values are sent serially to the PC. The computer calculates the temperature using Eq. 1. A Windows based software package provides a graphical interface to display the data, and allows the user to save data to disk. Figure 4 shows a functional block diagram of the decoder architecture.
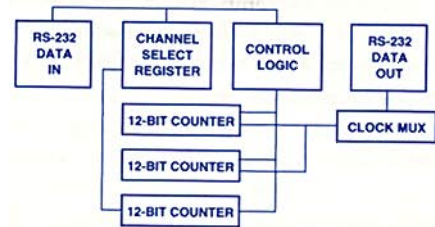

Figure 4. Evaluation board's decoder architecture.

These functional blocks were implemented in the programmable logic device (an ICT, Inc. PA7140 PEEL Array): sensor address registers for channel selection; two 12-bit timers (T_H and T_L quantization); serial data detection and synchronization, for transmission to the PC; output serial T_H and T_L count data; open/short sensor detector

A microcontroller could have been used, but the ICT PEEL Array offered distinct advantages as the system control device:

• Ease of development, prototype, simulation, and debugging, and lower cost of development and production.

• Precise control of timing in a deterministic, register-rich, parallel hardware architecture

• Eight sensors could be accommodated without external digital multiplexer. More channels are added by using the required number of digital multiplexers or programmable logic devices. For example, a 144-channel system would use 10 external PLDs, at an approximate additional parts cost of $.10 per channel..

The TMP03 provides the capability for an "easy-to-design" temperature acquisition system. With the low cost and ease of expansion of its multiplexed Evaluation Board, applications from remote industrial temperature sensing to home temperature sensing are now cost-effective because of the low cost-per-channel and ease of integration. Time to market is short because of the ease of design and specification.
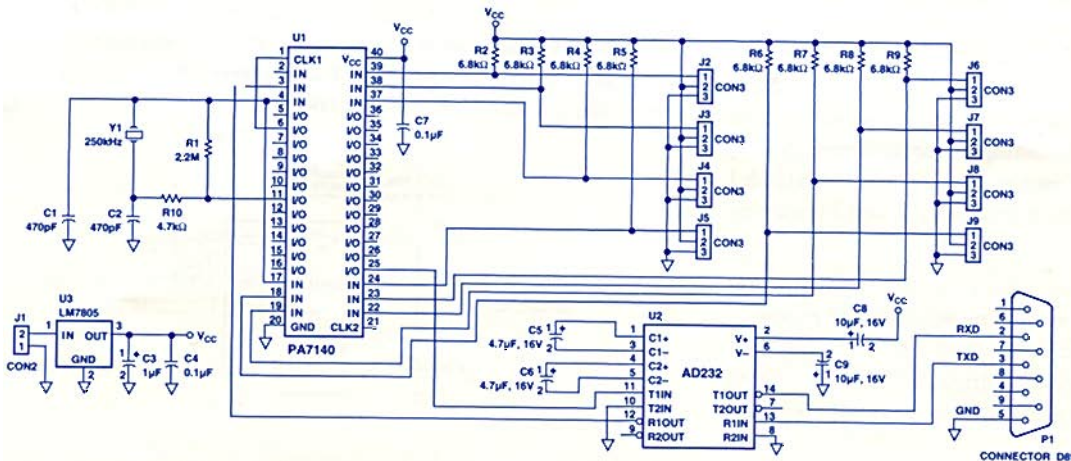
Figure 3. Block diagram of the TMP03 evaluation board.

Working with Batteries

- ## Measuring battery discharge power
- ## Controlled-power battery discharge
- ## Bypassing regulator at low voltage

Khy Vijeh

BATTERY DISCHARGE POWER AND ENERGY

When a battery is life-tested with a prescribed load, its terminal voltage may be a poor indicator of how much of its energy has been discharged. Figure 1 is a circuit of a wattmeter that uses an analog multiplier to measure the actual power (volts × amperes) being delivered by the battery at a given instant. To measure the total energy that has been delivered, the output voltage of the multiplier can either be integrated, using an analog integrator circuit with a very long time constant; or it can be sampled at frequent intervals by an A/D converter, with the Wh readings accumulated in a computer. Both discharge power and total energy can be displayed vs. time over the life of the battery.
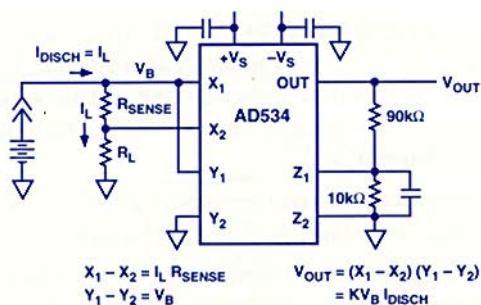

Figure 1. Using an analog multiplier to measure battery discharge power.

In the example of Figure 1, using an AD534 multiplier, with high-impedance differential inputs, the total load on the battery is $R_L + R_{SENSE}$. The voltage drop across R_{SENSE}, applied to the X input, measures the current through load R_L. The battery voltage, V_B, is applied to the Y input. The AD534's output is proportional to the battery's true instantaneous output power. Note that R_L could be an arbitrary linear or nonlinear grounded load circuit.

CONTROLLED-POWER DISCHARGE CIRCUIT

If you desire to measure the battery's terminal performance as it is being discharged at constant power, a power-measuring circuit like Figure 1 can be used in a feedback loop to enforce the constant power constraint. Figure 2 shows a circuit for discharging a battery at a controlled power level. The inset shows the basic scheme, in which the voltage output from the multiplier, representing power, (1 V corresponds to 1 W) is compared with a setpoint, and manipulates the discharge current to maintain power constant at the preset level.

Q1 should be selected to have the appropriate power-dissipation capability; a Darlington transistor could be used for higher power, but be sure to allow for V_{sat} of the Darlington. The error amplifier should have enough output current to drive the base of the pass transistor (an OP50 might be a good choice for high-current applications).
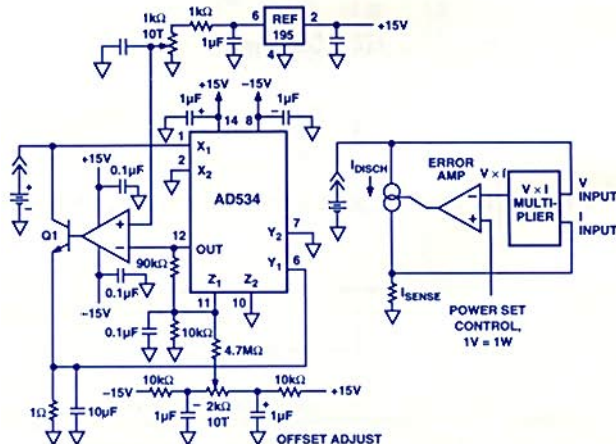

Figure 2. Controlled-power discharge circuit. The inset shows the basic feedback principle.

BYPASSING THE REGULATOR AT DROPOUT

One reason for using a voltage regulator is to maintain a constant voltage across the load at a level substantially less than a fresh, fully charged battery's terminal voltage, in order to minimize power dissipation in the load. As the battery is used, its output voltage gradually drops to a level where the regulator is no longer needed for voltage reduction. In fact, most regulators stop functioning when the voltage difference between the battery and load is reduced below a specified "dropout" level. Below this level, the regulator's output drops off sharply, effectively ending the usefulness of the circuit (even though the battery might still have sufficient capacity to feed the load by itself for a somewhat longer period).

To prevent this from happening, the battery voltage is monitored and a low-battery warning signal is issued, indicating the approaching end of battery life (and of regulator dropout). The circuit of Figure 3, using a regulator with low-battery warning capability, bypasses the regulator when low battery level is detected and connects the battery directly to the load circuit.

At high battery levels, the output voltage is regulated and the low-battery indicator is off; the LBO pin is pulled to the input level, and the power MOSFET is off. If the input level detector's reference (LBI) is set to $V = V_{out} + V_{sat}$ (of the regulator's pass transistor), using the ratio, $R_1/R_2 = V/1.3 V - 1$, then just as the regulator is on the verge of dropping out, LBO goes low, turning on the power MOSFET. From this point on, the output is the battery voltage less the insignificant MOSFET voltage drop. The important points to consider in selecting the MOSFET are its threshold voltage and R_{dson} resistance at this particular operating voltage. The circuit of Figure 3 will operate down to 2-V input with about 150 mV dropout at 100 mA. ▶
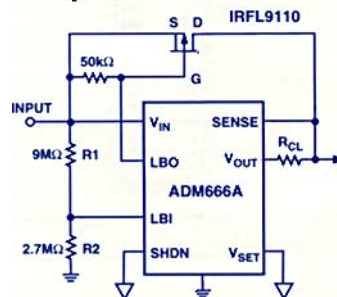

Figure 3. Bypassing the regulator when it drops out of regulation.

Single-Chip PC Sound System

AD1812 SoundPort® controller integrates DSP and codec, supports PC standards, simplifies motherboard

by David Babicz

The AD1812*SoundPort Controller is a single-chip audio sub-system for adding 16-bit stereo audio to personal computers. The ISA Plug and Play (PnP) system is compatible with applications written for Windows 95, the Microsoft Windows® Sound System, Sound Blaster Pro® and Ad Lib®, and provides an MPU-401 compatible interface and a game port complete with timer.

ISA PnP Interface: The chip is complete with all necessary ISA PnP bus interface logic. This includes address decoding for all on-board resources, control and signal interpretation, DMA selection and control logic, IRQ selection and control logic, and all interface configuration logic. The AD1812 can support one, two, or three DMA channels. Included are dual DMA count registers for full-duplex operation, enabling simultaneous capture and playback on separate DMA channels. The AD1812 is fully configurable according to the Plug and Play ISA Specification. Table 1 lists the logical devices supported by the AD1812 that are ROM coded in its PnP space. For a non-Plug and Play environment, the built in PnP services allow the AD1812 to operate under a user-defined fixed address space.

Table 1. Emulated Logical Devices

Logical Device Number	Emulated Device
0	Windows Sound System
1	Sound Blaster Pro v.2.01
2	OPL3 Music Synthesizer
3	MIDI MPU-401 Port
4	Game/Joystick Port
5	Modem

Codec: The built-in 16-bit SoundPort® Stereo Codec supports business audio and multimedia applications. The codec includes stereo audio converters, complete on-chip filtering, an MPC Level-2-compliant analog mixer, and FIFOs for buffering the ISA bus. The pair of 16-bit outputs from the ADCs are available over a 16-bit bidirectional interface that also supplies 16-bit digital data to the DACs. The codec can accept and generate 16-bit twos-complement PCM linear (big-endian or little-endian) digital data, 4-bit IMA-ADPCM compatible digital data, 8-bit unsigned magnitude PCM linear data, and 8-bit μ-law or A-law companded digital data..

Multimedia Support: The SoundPort Controller combines an embedded 16-bit fixed-point Analog Devices signal processor and dedicated hardware to emulate all Sound Blaster version 2.01 functions. The ROM-coded music synthesis algorithms imitate industry-standard OPL3 FM synthesizer chips and can deliver 20 voice polyphony.

MPU-401: The primary interface for communicating MIDI data to and from the host PC is the emulated MPU-401 interface, which includes a built-in FIFO for communicating to the host bus.

Game Port: The chip includes an IBM-compatible game port interface, capable of supporting up to two joysticks. Connecting the game port to a 15-pin D-sub connector requires only a few capacitors and resistors.

Systems Are Easy To Build: The AD1812 has everything needed for a PnP audio controller and in a form more integrated than one might expect. The internal PnP services can decode up to 6 logical devices for designing seamlessly integrated subsystems. No known audio controller offers as much!
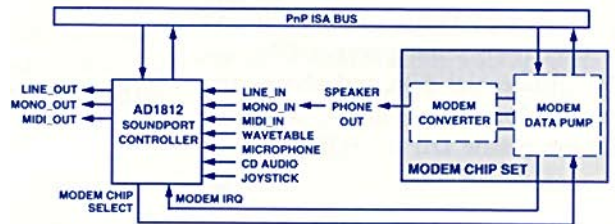

Figure 2. Audio/telecom PnP ISA system

Functioning as more than just a codec, the AD1812 enables multimedia and telephony in any PC. When coupled with a modem chip set, the subsystem can provide 16-bit sound support for popular DOS games and Windows 95 audio applications, fax, full-duplex speaker phone, and a high-speed modem. For even more realistic music, a Wavetable synthesizer's output can be mixed with the Wave audio converted by the on board DACs.

As an aid to the designer, Analog Devices offers reference designs for the AD1812 & modem chip set, and the AD1812 & Wave Blaster header. Device drivers are available for Windows 95, Windows 3.1x, Windows NT, and OS/2.

Availability: The AD1812 is available for 0 to +70°C in 160-pin plastic quad flat pack (PQFP) and thin quad flat pack (TQFP) packages.

The AD1812 analog design team was led by Bob Libert, at Wilmington MA; the digital design team was led by John Amann, and the software team by Chris Russell, at Norwood MA.
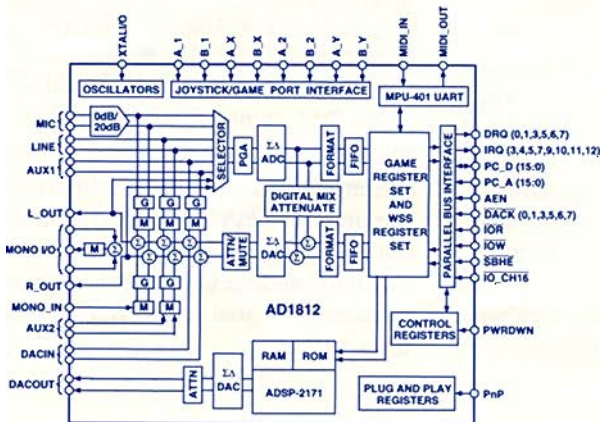
Figure 1. AD1812 block diagram.

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Multiple Amplifiers—High Speed, Low Power

Triple Video Op Amp
AD8013: Low power, high cap. load drive, Disable

The monolithic AD8013 comprises 3 low-power, single-supply, current-feedback wideband amplifiers, each capable of driving 30 mA of output current. It is optimized for systems that require the ability to drive capacitive loads, yet settle rapidly while heavily loaded. Other applications are in RGB video systems driving 150-Ω back-terminated lines.

The device operates on single or dual supplies (5 to 13 V between rails), with 4 mA of quiescent current per amplifier—and 30-ns power-down for a further ×10 current reduction, with high-impedance output. Specs include 140-MHz BW (0.1 dB flatness to 60 MHz), 1000-V/μs slew rate, 18-ns settling time, 0.02% and 0.06° differential gain and phase, and 95-mA I_{sc}. Operation is from –40 to +85°C, in 14-pin plastic DIP or SOIC.

▶

Wideband Rail-to-Rail Dual and Quad
AD8042 and AD8044 are 150-MHz V-feedback amps Spec'd for +3, +5, and ±5 V; 0.04%/0.06° $\Delta G/\Delta\phi$

The AD8042/AD8044 (dual/quad) are wideband voltage-feedback operational amplifiers with a +3 V to ±6 V supply range. In single-supply operation, the input can swing below ground. Typical applications are in video, high-speed data modems, and wireless-communication. Packaging is in 8- or 14-pin plastic DIP or SOIC; specified operating temperature is –40 to +85°C. ▶

### Typical Characteristics, AD8042 and AD8044

Supply voltage	+3 V		+5 V		±5 V	
AD804xA (x = no. of devices)	2	4	2	4	2	4
Bandwidth, –3 dB, MHz	140	135	160	150	170	160
0.1-dB flatness, MHz	14	10	11	12	18	15
Slew rate, V/μs	170	150	200	170	225	190
Settling time (0.1%), ns	45	55	39	40	32	30
THD (dBc)	–56	–54	–73	–75	–78	–77
Diff. gain error (NTSC)	0.1%	0.13%	0.04%	0.04%	0.02%	0.06%
Diff. phase error (NTSC)	0.12°	0.3°	0.06°	0.22°	0.04°	0.15°
Δswing, 10 kΩ (±V_s–FS) mV	30, –30	25,–20	30,–30	30,–25	30,–30	30,–30
I_{sc}: sourcing, sinking, mA	50, 70	30, 50	90,100	45, 85	100,100	60,100
Quiescent current, mA max	12	12.5	12	13.1	14	13.6

Dual μPower Op Amp
60 μA/amplifier, OP296 Rail-rail input & output

The monolithic OP296 is a pair of micropower single-supply op amps with rail-to-rail input *and* output. It has low offset (300 μV max), up to 450 kHz of bandwidth, and it consumes only 60 μA per amplifier. With its low power requirements and guaranteed operation from +3 to +12 V, it is well-suited to operation from (and instrumentation of) batteries. Excellent dynamics and low noise (26 nV/√$\overline{Hz}$) recommends it for battery-powered audio applications. It can handle capacitive loads of up to 200 pF without oscillation.

The input CMV range is equal to the supply; the output swings to <150 mV of the positive rail and <70 mV of ground. Temperature specs are 0 to +125°C (3 V) and –40 to +125°C (≥4 V). Packaging is in 8-pin plastic DIPs and SOICs (TSSOPs soon).

▶

Quad Current-Feedback Amplifier
AD8004 uses 70 mW, has 3000 V/μs slew rate 130-MHz full-power BW, low THD (–78 dBc at 5 MHz)

The monolithic AD8004, with its four low-power, high-speed current-feedback amplifiers, can be used to amplify, buffer, or condition any high-speed signal in systems where power and space are at a premium. Fully specified for operation at +5 V single-supply (3.5 mA max per amplifier) and ±5 V dual supply, it will operate on any supply rails from 4–12 V.

Among low-power, low-price amplifiers, the AD8004 stands out in dynamic performance, with its low distortion (–78 dBc at 5 MHz), high full-power bandwidth (130 MHz), wide flatness bandwidth (30 MHz for 0.1%), high slew rate (3000 V/μs), short settling time (21 ns to 0.1%), and low noise (1.5 nV/√$\overline{Hz}$). For video applications, such as cameras and switchers, its differential gain- and phase-error specs are 0.06% and 0.25° with 150-Ω load, dropping to 0.01% and 0.08° with 1 kΩ.
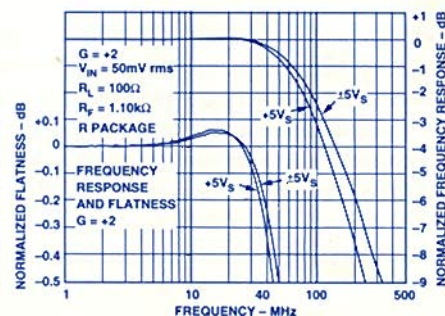
The amplifiers can furnish 50 mA of output current and have available a short-circuit current of 100 mA (minimum) for transient loads. The AD8004 is available in 14-pin DIP and SOIC packages, with operation over the extended industrial temperature range of –40 to +85°C.

▶

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Four A/D Converters and a Complete 3-V Serial DAC

16/12-Bit High-Speed Σ-Δ ADC
AD7721 is *fast*: 468.75-kHz output word rate
Input bandwidths up to 229.2 kHz; Uses +5-V supplies

The monolithic AD7721 is a complete ratiometric low-power 16-bit serial (12-bit parallel) sigma-delta A/D converter with serial output word rates up to 468.75 kHz (0.1-15-MHz clock). It operates on a +5-volt supply and accepts single-ended (0 to 2.5 V) or differential (±1.25 V) inputs with bandwidths up to 229.2 kHz. The antialiasing filter (if required) can be a simple first-order RC. The serial output port allows easy interfacing to industry-standard µCs, µPs, and DSPs.

The AD7721 employs a high-order Σ-Δ modulator with differential inputs, which produces an oversampled digital pulse train at the clock frequency with most of the quantization noise concentrated at the high frequencies. It is followed by two cascaded FIR digital filters, which convert the pulse train into 12- or 16-bit-wide binary data, and reduce the data rate from f_{CLK} to $f_{CLK}/32$
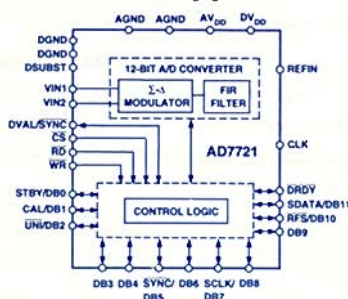
(e.g., from 15 MHz to 468.75 kHz). In either mode, the minimum no-missing-codes resolution at maximum clock frequency is 12 bits.

Power required at 5 V (±5%) is 150 mW (max) in active mode, 100 µW standby. Packaging is a 28-pin plastic DIP or SOIC (A: –40 to +85°C) or cerdip (S: –55 to +125°C).

▶

Mux'd 12-Bit ADC
500-kSPS-thruput AD7891
8 channels, single 5 V supply

The monolithic AD7891 is a 12-bit data-acquisition system consisting of a sampling A/D converter with an internal 2.5-V reference, an 8-channel multiplexer, and selectable serial or parallel output. Operation is from a single 5-volt supply, and conversion time is 1.6 µs max. Two versions provide a variety of *bipolar* and single-ended analog input ranges: AD7891-1 handles ±5 and ±10 V with 0.6-µs max acquisition time, and AD7891-2 accquires 0 to +2.5 V, 0 to +5 V, and ±2.5-V in 0.4-µs max.

The AD7891 can withstand overvoltage to ±17 V on an unselected channel without affecting a selected channel. Dissipation at +5 V is 85 mW max in normal mode, and 150 µW max in Standby. Packaging for –40 to +85°C operation is in 44-lead PLCC and PQFP.

▶

12-B, 10-MSPS ADC
AD9220: complete, 250-mW
+5-V; 88-dB SFDR @ 1 MHz

The AD9220 is a monolithic, single-supply, 12-bit-10-MSPS sampling analog-to-digital converter with an on-chip voltage reference. 12-bit resolution, and no missing codes, is guaranteed over the entire –40 to +85°C operating temperature range. Its high-performance sample-hold amplifier will accept either differential or single-ended analog signals, and the voltage reference is programmable for either 1.0 or 2.5 V. Excellent dynamics include full-power bandwidth of 50 MHz, Sinad of 68.5 dB min at 1 MHz and 65 dB min at 4.99 MHz. Its many applications in communications and instrumentation include base stations, imaging, analyzers, ultrasound, etc.

It requires only 250 mW at 5 V, operates from –40 to +85°C, and is housed in a 28-pin, 0.3" SOIC.

▶

11-Bit 7-Channel A/D
Simultaneous sampling
AD7861 for control & comm.

The AD7861, an 11-bit multichannel ADC, has features and performance to implement a low-cost solution in a variety of applications, including motor control, 3-phase power systems, and general-purpose data acquisition. It samples 4 channels simultaneously, and conversion data can be read out in any sequence via double-buffered registers. One channel offers a choice among 4 auxiliary inputs.

Conversion time is 3.2 µs per channel, and acquisition time is 1.6 µs per group. The AD7861 logic and interface are compatible with microcontrollers and ADI's ADSP-21xx series of fixed-point DSPs. The AD7861 dissipates only 85 mW with a 5-V supply, operates from –40 to +85°C, and is packaged in a 44-lead PLCC.

▶

+3 V, Dual 12-Bit D/A
Serial in, rail-to-rail output
AD8303 fits in narrow SO-14

The AD8303 is a +3-V complete two-channel single-supply 12-bit D/A converter packaged in a space-saving SO-14 narrow-body surface-mount package. Its outstanding accuracy (resolution of 12 bits at +3 V!) includes 3/4-LSB differential nonlinearity, ±2-LSB integral nonlinearity, and ±8.5-mV full-scale error. Complete and ready-to-use, it includes a pretrimmed internal reference with a 16 ppm/°C tempco.

It eliminates headroom requirements with a rail-to-rail output design allowing specified operation with a 2.7-V supply. It can operate on a single lithium battery cell and has a 1-µA Shutdown mode. SPI-compatible serial input-data loading can be clocked in excess of 12.5 MHz. Also available in PDIP, it operates from –40 to +85°C.

▶

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Mixed Bag #1: Regulate, Refer, Switch, Compare, Mix

1.2-V Reference
μpower AD1580 in SOT-23
±0.1%, 50 ppm/°C, 50 μA

The AD1580 is a low-cost micropower two-terminal high-precision shunt voltage reference. The first *high-precision* reference to be housed in a tiny SOT-23 surface-mount package, it is designed for applications in the computer, automotive, communications, and instrumentation industries. It is especially suitable for portable 3- and 5-volt designs, where low power and a small footprint are essential.

It offers a stable, accurate 1.225-V (nominal) output over a range of operating currents from 50 μA to 10 mA. Specified over the industrial temperature range, –40 to +85°C, it operates at temperatures up to 125°C. It is available in B & A grades with initial tolerances of 1 mV & 10 mV, drift specs of 50 & 100 ppm/°C, and max dynamic output impedance of 0.5 ohm & 1 ohm.

▶

8-Channel Audio Mixer
SSM2163: Digital volume control, 63 1-dB steps
Low noise (–82 dBu)-and-distortion (0.007%)

The SSM2163, a complete stereo-output monolithic mixer, accepts 8 audio inputs, controls the volume of each in sixty-three (63) 1-dB steps, and adds each input to the right, left, or both outputs under digital control.

A complete voltage-input, voltage-output mixer on a single chip, it requires no external active components. It uses a standard 3-wire serial interface, and includes a Data Out terminal; this facilitates daisy chaining with additional mixer ICs to increase the number of channels.

Performance includes –82 dBu of signal-to-noise ratio (0 dBu = 0.775 V rms), +10 dBu of headroom, and total harmonic distortion-plus-noise (THD+N) of 0.007% at 1 kHz, unity gain, 0 dBu.

The SSM2163 can operate on ±4 to ±7 V (dual) or +5 to +15 V (single) supplies.

DCA: DIGITALLY CONTROLLED ATTENUATOR
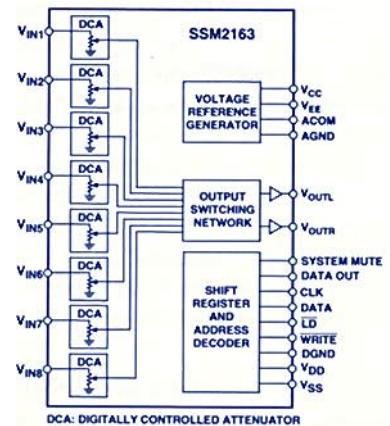
Typical applications include multimedia system mixing, audio mixing consoles, broadcast equipment, intercom/paging systems, and musical instruments. It is available in 28-pin plastic DIP and SOIC packages, with a range of –40 to +85°C.

▶

Lo-Dropout Regulator
ADP3367: Fixed (5 V ± 2%)
or Adjustable: 1.3 to 16.5 V

The ADP3367 is a low-dropout precision voltage regulator that can supply up to 300 mA of output current with just 500 mV of headroom. It draws as little as 30 μA max of quiescent current (at 0.1 mA), and this can be further reduced to 0.75 μA max in a power-conserving Shutdown mode; also featured are low-battery and dropout detection. These are all useful features in notebook and palmtop computers, pagers, and other battery-operated equipment.

The ADP3367 has 6 kV of ESD protection. It can provide a fixed 5-volt (±2%) output or an adjustable 1.3-to-16.5-volt output range, with an input range of 2.5 to 16.5 volts. Housed in a narrow 8-lead low-thermal-resistance SO package, the ADP3367AR operates from –40 to +85°C.

▶

Quad SPDT Switch
ADG333A has <45-Ω R_ON,
Rail-to-rail signal range

The monolithic ADG333A comprises four single-pole, double-throw break-before-make switches, and is available in 20-pin DIP, SOIC, and SSOP packages. Its small SSOP package and low power dissipation make it suitable for a wide range of applications, including multiple two-channel multiplexing in portable, battery-powered instruments. It is pin-compatible with other 333A devices.

The ADG333A handles rail-to-rail signals. Key features include low R_{on} (<45 Ω, –40 to +85°C), low supply current (0.35 mA max over temperature), and low leakage (±3 nA max OFF and ±5 nA max ON over temperature). The power supply range is from ±3 V to ±20 V, or +3 V to +30 V (single-supply), and the device has a 4-kV ESD classification.

▶

Quad Comparators
CMP401/402: 23/65 ns
Work with 3 or 5-V supplies

The CMP401/402 have 4 comparators on a single monolithic chip. The CMP401 is the faster device, with 23-ns max propagation delay (100-mV step with 20-mV overdrive), compared to 65-ns prop delay for the CMP402. Accordingly, the CMP401 requires greater analog supply current, 6.5 mA max, compared to 2.25 mA. Otherwise, they are similar.

The input and output stages have separate supply terminals, allowing a range of analog supplies, from +3 V to ±6 V, to be used with standard 3- or 5-volt digital logic supplies. With +5-V supplies, the offset voltage is 4 mV max (–40 to +125°C). Outputs can be toggled at 20 MHz with only 100-mV overdrive. The devices are available in 16-pin plastic DIP & narrow SOICs, and 16-lead TSSOPs.

▶

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Mixed Bag #2: Drive Current, Control Temp & Motion, Convert DC/DC

Airflow, Temperature
TMP12 monitors airflow in cooling systems

The TMP12 comprises a heating resistor, a linear temperature sensor, and a pair of setpoint comparators with hysteresis. When the TMP12 is placed in a cooling airstream, the heat it generates is conducted away and its temperature tends to decrease. Its sensor and the setpoint comparators determine whether the device's temperature is within a user-set window—allowing it to provide a warning of cooling system failure or feedback information to control the airflow. Typical applications are in monitoring and control of temperature in fan-cooled equipment, such as computers and power supplies.

The TMP12 operates from a single +5-V supply, at ambients from −40 to +150°C, and measures temperature to within about ±3°C from −40 to +100°C. It is packaged in 8-pin plastic DIP and SO.

▶

Thermostatic Switch
AD22105: Low voltage, resistor programmable

The AD22105 is a low-cost, general-purpose, easy-to-use, compact monolithic thermostatic switch designed for a wide range of single setpoint applications. It combines a temperature sensor, an open-collector output stage, and a setpoint comparator with hysteresis, programmed by a single external resistor. It can switch at any temperature from −40 to +150°C.

Its wide variety of applications includes process control and thermal management. Maximum error is ±2° at 25°C, and ±3° over the whole range. Hysteresis, to prevent rapid on-off cycling, is preset at about 4°C. The single-supply AD22105 operates from +2.7 to +7 V; dissipation is only 230 μW at 3.3 V to minimize self-heating and maximize battery life in portable systems. It is packaged in an 8-lead plastic SOIC.

▶

Motion Coprocessors
Interface circuitry to motors, Perform vector transforms

The monolithic ADMC200 and ADMC201 motion coprocessors can be used with DSPs or microcontrollers for servo or variable-speed control of permanent-magnet synchronous or ac induction motors. The coprocessors are also available in chipsets with ADI DSPs.

An on-chip 4-channel simultaneous-sampling ADC (like the AD7861, p. 17) samples 3-phase currents with minimal relative phase error. The chip performs Clarke and Park vector transformations and generates PWM drive signals. An embedded control sequencer offloads the DSP or μP, reducing the instruction burden and freeing the host processor for performing control algorithms.

The **ADMC201** includes a 6-bit digital I/O port and a 4-channel AUX mux input. Both products operate from −40 to +85°C and are available in a 68-pin PLCC.

▶

Fast Si Laser Driver
AD9661A controls light power for copiers & printers

The AD9661A is a highly integrated driver for laser-beam printers and copiers. It combines a fast output-current switch with an on-chip analog light-power control loop to improve the user's control over the final document image. The AD9661A features fast rise and fall times (1.5 ns typical, 2 ns max) and 200 MHz pulse rates. Fast switching is important in laser-beam printer applications, because of fast page rates (10-30 pages/min), high-resolution printing (600-1200 dpi), and pulse-width modulation to enhance images and text.

The AD9661 uses a +5-V supply and provides up to 120 mA to an IR N-type laser. An analog feedback loop is used for calibration—but it can also be used for operation at rates up to 25 MHz. The device is housed in a 28-pin plastic SOIC, operates from 0 to 70°C

▶

Differential Driver
AD815 amplifier pair drives 500 mA for telecomm, CRTs

The AD815 consists of two high-speed current-feedback amplifiers capable of supplying ≥500-mA. They can be used independently, but in a typical application, they are configured as a differential driver capable of 40 V p-p using ±15-V supplies. Low distortion, wide bandwidth, and high current drive make the device ideal for communication applications, such as subscriber line interfaces for ADSL, HDSL, and VDSL.

As a video distribution amplifier, the AD815 can drive 12 back-terminated loads, while keeping differential gain and phase errors to 0.05% and 0.45°. The device is protected by automatic thermal shutdown when overloaded. The AD815 is available in suitable power packages to dissipate generated heat and will operate from −40 to +85*C.

▶

DC-DC Converter
28 V in, 5 V out @ 100 W Has integral EMI filter

The ADDC02805SA is a high-density 100-W dc-to-dc converter from 28 V dc to 5 V dc @ 20 A, using a 1-MHz (effective) switching frequency. The integral filter for differential and common-mode EMI is designed to meet all applicable requirements of MIL-STD-461D when installed in a typical system setup.

The many protection and system-level features eliminate costly external circuits. With thermal shutdown, protection against input transient/overvoltage and output short-circuit/overvoltage—and system-level features, such as current-share, inhibit, and status, it can be used as a component in a larger system or as a standalone supply. Housed in a hermetic hybrid package, available grades include commercial, ruggedized industrial, and (soon) /883B.

▶

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Ask The Applications Engineer—20

INTERFACING TO SERIAL CONVERTERS—II

by Eamon Nash

Q. *At the end of our discussion in the last issue, I was having a problem establishing communication between my ADC and my microcontroller. If you recall, the microcontroller always seemed to be reading a conversion result of FFF_{HEX} regardless of the voltage on the analog input. What could be causing this?*

A. There are a number of possible timing-related error sources. You could start trouble-shooting this problem by connecting all of the timing signals either to a logic analyzer or to a multi-channel oscilloscope (at least three channels are needed to look at all signals simultaneously). What you would see on the screen would look similar to the timing diagram in the figure below. First make sure that a Start Conversion command (CONVST) is being generated (coming either from the micro or from an independent oscillator). A frequent mistake is to apply a CONVST signal with the wrong polarity. The conversion is still performed, but not when you expect it to be. It is also important to remember that there is usually a minimum pulse width requirement on the CONVST signal (typically about 50 ns). The standard Write or Read pulse from fast microprocessors may not satisfy this requirement. If too short, the pulse width can be extended by inserting software Wait states.
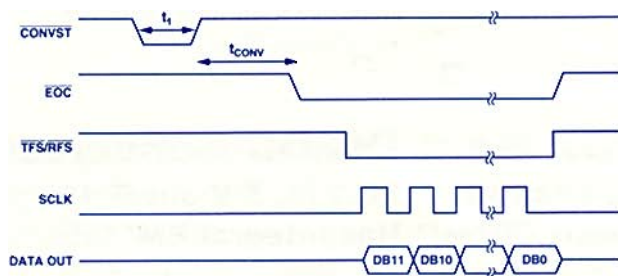

Make certain that the micro is waiting for the conversion to be completed before the Read cycle begins. Your software should either be taking note of the time required to convert or be waiting for an End of Conversion (EOC) indicator from the ADC to generate an interrupt in the micro. Make sure that the polarity of the EOC signal is correct, otherwise the ADC will cause an interrupt while the conversion is in progress. If the micro is not responding to the interrupt, you should examine the configuration of the interrupt in your software.

It is also important to consider the state of the serial clock line (SCLK) while it is not addressing the converter. As I mentioned in our previous discussion, some DACs and ADCs do not operate correctly with continuous serial clocks. In addition to this, some devices require that the SCLK signal always idles in one particular state.

Q. *O.K. I've found and corrected some bugs in my software and things seem to be improving. The data from the converter are changing as I vary the input voltage but the conversion results seem to have no recognizable format.*

A. Once again there are a number of possible error sources. The ADC will be outputting its conversion result either in straight binary or in twos complement format (BCD data converters are no longer widely used). Check that your micro is configured to accept the appropriate format. If the micro can't be configured to accept twos complement directly, you can convert the data to straight binary by exclusive-or'ing the number with 100 . . . 00 binary.

Normally the leading edge of the serial clock (either rising or falling) will enable the data out of the ADC and onto the data bus. The trailing edge then clocks the data into the micro. Make sure that both micro and ADC are operating under the same convention and that all Setup and Hold times are being met. A conversion result that is exactly half or double what one would expect is a tell-tale sign that the data (especially the MSB) is being clocked on the wrong edge. The same problem would manifest itself in a serial DAC as an output voltage that is half or double the expected value.
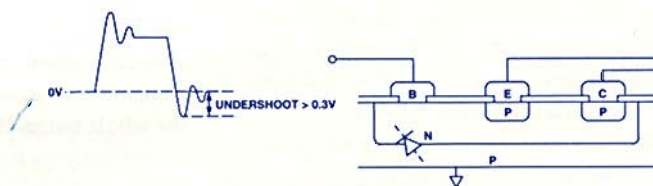

The digital signals driving the converter should be clean. In addition to causing possible long-term damage to the device, overshoot or undershoot can cause conversion and communication errors. The figure shows a signal with a large overshoot spike driving the clock input of a single-supply converter. In this case, the clock input drives the base of an PNP transistor. As is usual practice, the P-type substrate of the device is internally connected to the most negative potential available—in this case, ground. An excursion of more than 0.3 volts below ground on the SCLK line is sufficient to begin turning on a parasitic diode between the N-type base and the P-type substrate. If this happens frequently, over the long term, it may lead to damage to the device.

In the short term, though not causing damage, energizing the normally inert substrate affects other transistors in the device and can lead to multiple clock pulses being detected for each pulse applied. The resulting jitter is a serious matter in serial converters—but is less of a problem in parallel converters, because the Read and Write cycles generally depend upon the first applied pulse; subsequent pulses are ignored. However, the noise performance on both serial and parallel converters can suffer if signals of this kind are present during conversion.

The figure shows how overshoot can be easily reduced. A small resistor is placed in series on the digital line that is causing the problem. This resistance will combine with C_{par}, the parasitic capacitance of the digital input, to form a low-pass filter which should eliminate any ringing on the received signal. Typically a 50-Ω resistor is recommended, but some experimentation may be necessary. It may also be necessary to add an external capacitance from the input to ground if

the internal capacitance of the digital input is insufficient. Here again, experimentation is necessary—but a good starting point would be about 10 pF.
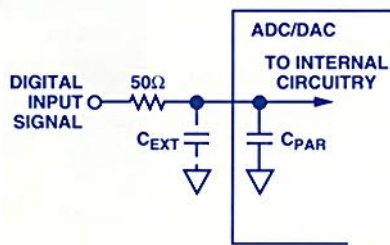
Q. *You mentioned that clock overshoot can degrade the noise performance of a converter. Is there anything else I can do from an interfacing point of view to get a good signal to noise ratio?*

A. Because your system is operating in a mixed-signal environment (i.e., analog and digital), the grounding scheme is critical. You probably know that—because digital circuitry is noisy—analog and digital grounds should be kept separate, joined at only one point. This connection is usually made at the power supply. In fact, if the analog and digital devices are powered from a common supply, as might be the case in a +5 V or +3.3 V single-supply system, there is no choice but to connect the grounds back at the supply. But the data sheet for the converter probably has an instruction to connect the pins AGND and DGND at the device! So how can one avoid creating a ground loop that can result if the grounds are connected in two places?

The figure below shows how to resolve this apparent dilemma. The key is that the AGND and DGND labels on the converter's pins refer to the parts of the converter to which those pins are connected. The device as a whole should be treated as *analog*. So after the AGND and DGND pins have been connected together, there should be a single connection to the system's analog ground. True, this will cause the converter's digital currents to flow in the analog ground plane, but this is generally a lesser evil than exposing the converter's DGND pin to a noisy digital ground plane. This example also shows a digital buffer, referred to digital ground, to isolate the converter's serial data pins from a noisy serial bus. If the converter is making a point-to-point connection to a micro, this buffer may be unnecessary.
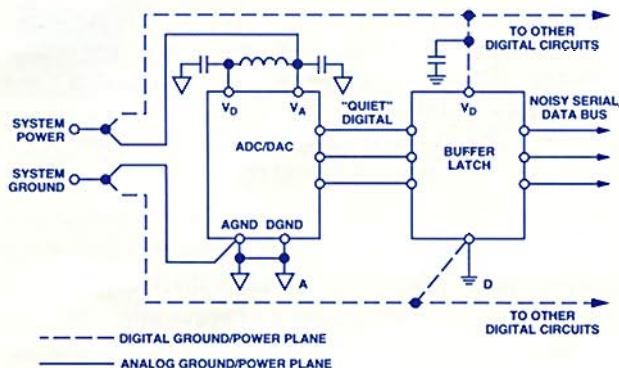
The figure also shows how to deal with the increasingly common challenge of powering a mixed-signal system with a single power supply. As in the grounding case, we run separate power lines (preferably power planes) to the analog and digital portions of the circuit. We treat the digital power pin of the converter as analog. But some isolation from the analog power pin, in the form of an inductor, is appropriate. Remember that both power pins of the converter should have separate decoupling capacitors. The data sheet will recommend appropriate capacitors, but a good rule of thumb is 0.1 μF. If space permits, a single 10-μF capacitor per device should also be included.

Q. *I want to design an isolated serial interface between an ADC and a microcontroller using opto-isolators. What should I be aware of when using these devices?*

A. Optoisolators (also known as opto-couplers) can be used to create a simple and inexpensive high-voltage isolation barrier. The presence of a galvanic isolation barrier between converter and micro also means that analog and digital system grounds no longer need to be connected. As shown in the figure, an isolated serial interface between the AD7714 precision ADC and the popular 68HC11 microcontroller can be implemented with as few as three optoisolators.
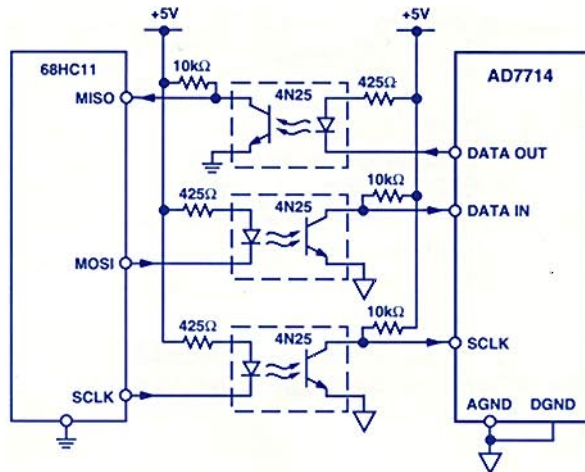
The designer should be aware, though, that the use of optoisolators having relatively slow rise and fall times with CMOS converters can cause problems, even when the serial communication is running at a slow speed.

CMOS logic inputs are designed to be driven by a definite logic zero or logic one. In these states, they source and sink a minimal amount of current. However, when the input voltage is in transition between logic zero and logic one (0.8 V to 2.0 V), the gate will consume an increased amount of current. If the opto-isolators used have relatively slow rise and fall times, the excessive amount of time spent in the dead-band will cause self-heating in the gate. This self-heating tends to shift the threshold voltage of the logic gate upwards, which can lead to a single clock edge being interpreted by the converter as multiple clock pulses. To prevent this threshold jitter, the lines coming from the optoisolators should be buffered using Schmitt trigger circuits, to deliver fast, sharp edges to the converter. ▶

Worth Reading

SPICE LIBRARY UPDATE

ADSpice Library Release "L", January, 1996. Total of 550 macromodels includes 105 new models and 33 generics on a 3.5" diskette. **FREE.**

BROCHURES AND GUIDES

High-Speed Signal-Processing Solutions, a 16-page guide to high-speed IC products and applications. Includes **signal chains** for scanners, medical imaging, cellular basestations, set-top boxes, and high-speed 12-bit systems; a set of 12 **general high-speed circuit solutions; product highlights**, and a **Selection Guide. FREE**

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AD1843 Serial-Port 16-bit SoundComm® Codec, 64-page comprehensive technical data.

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APPLICATION NOTES

Overcoming converter nonlinearities with dither, by Brad Brannon [8 pp., AN-410]. Defines dither and explains how it can be applied to improve ADC linearity. Examples are given using the AD9042 12-bit, 41-MSPS ADC.

An outboard digital-to-analog converter for digital audio sources, by Hank Zumbahlen [12 pp., AN394]. Describes the design and theory of operation of a complete audio D/A converter, including AES/EBU receiver, asynchronous sample-rate converter, interpolation filter, DAC, reconstruction filter, output driver, and power supply.

Interfacing the AD1890/AD1891 to AES/EBU receivers and digital filters, by Hank Zumbahlen [2 pp. AN399]. This application "brief" discusses the issues in using AD1890 and AD1891 asynchronous sample-rate converters when interfacing digital audio components in the digital domain.

Acceleration to frequency circuits, by Charles Kitchin, Dave Quinn, and Steve Sherman [4 pp., AN-411]. Combining accelerometers with V/f converters to get the advantages of transmitting analog info as frequency.

Replacing output clamping op amps with input clamping amps, by Peter Checkovich [4 pp., AN-402]. Discusses advantages of input clamping over output clamping; shows circuitry for inverting and non-inverting applications.

Increasing the speed of the output response of the AD606 (demodulating log amplifier), by Peter Checkovich [4 pp., AN-405]. Describes schemes for obtaining an eightfold increase in output speed of a complete demodulating log amplifier by bypassing the output filter.

Evaluation boards for single, dual, and quad operational amplifiers, by Adolfo A. Garcia [6 pp., AN-398, revised 1/96]. Describes evaluation boards for quick and easy evaluation of precision and medium-speed (<10-MHz GBW) op amps in inverting and non-inverting applications—including evaluation and compensation for effects of capacitive loading. ▶

MORE AUTHORS [Continued from page 2]

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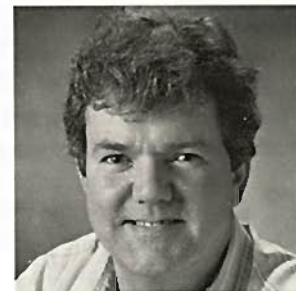
Khy Vijeh (page 14) is an Applications Engineer for ADI's Power-Management Group in Santa Clara, CA. Khy has a BSEE. Prior to joining Analog Devices, he held various engineering and management positions with high-tech and startup companies in Silicon Valley. In his spare time, he enjoys traveling with his family, growing rare plants, biking, backpacking, music, and home-improvement projects.

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An Eclectic Collection of Miscellaneous Items of Timely and Topical Interest. Further Information on Products Mentioned Here May Be Obtained Via the Reply Card.

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D/A Converter, 16-bit, 4-to-20 mA,
loop-powered AD421
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A/D Converter, 9-bit, 30 MSPS, +3, +5-V
single supply AD9049
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200 ksps/100 ksps AD7859/59L
Switch, Dual SPDT, high performance, 12 Ω, 5 pA .. ADG436
ADSL Chip set, ANSI T1.413-compliant AD6444

ERRATA, etc. • • • A revised and updated version of the **Single Supply Amplifier Guide** is available • • • A **revised ADXL50 specification sheet** is available with minor changes (new Self-Test limits are −0.85 to −1.15 V).

STANDARDS AND MILITARY • • • The **16-bit, 100-ksps AD677 A/D** converter is now available for **both /883 and SMD specifications**: AD677TD/883B and SMD 5962-9559201MEA • • • **Two Analog Devices manufacturing sites** (Wilmington, MA, and Limerick, Ireland) have **received QS-9000 conformance certificates as suppliers to U.S. automobile manufacturers** from Delco Electronics, a tier-one supplier to GM; and a third site—in Santa Clara, CA—is in process. Quality Specification **(QS) 9000 was developed by GM, Ford, and Chrysler** to establish new standard practices for the automotive industry. **QS-9000 incorporates the ISO 9000 quality standards—and in addition, it includes previous industry standards and Advanced Product Quality standards**, such as Failure Modes Effects Analysis (FMEA) and Gauge Repeatability and Reproducibility to anticipate and prevent potential problems • • • **Our Greensboro (NC) site has received an ISO-9001 Letter of Conformance** from DESC, following a Mil-PRF-38534 biannual audit and an ISO-9001 Quality System audit.

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PATENTS • • • 5,432,478 to Barrie Gilbert for **Linear interpolation circuit** • • • 5,453,710 to Barrie Gilbert and Shao-Feng Shu for **Quasi-passive switched-capacitor (SC) delay line** • • • 5,461,343 to Ryan P. Foran for **Current mirror circuit** • • • 5,465,604 to Steven J. Sherman for **Method for adjusting sensitivity of a sensor** • • • 5,467,009 to Gerard F. McGlinchey for **Voltage regulator with multiple fixed plus user-selected outputs** • • • 5,467,044 to James Ashe and Derek F. Bowers for **CMOS input circuit with improved supply voltage rejection** • • • 5,469,113 to Michael Steyaert, Wim Dehaene, Jan Craninckx, Mairtin Walsh, and Peter Real for **Rectifier and integrator circuit for disk-drive servo system** • • • 5,471,411 to Robert W. Adams, Tom W. Kwan, and Michael Coln for **Interpolation filter with reduced set of filter coefficients** • • • 5,471,607 to Douglas Garde for **Multi-phase multi-access pipeline memory system** • • • 5,475,628 to Robert W. Adams, Tom W. Kwan, and Michael Coln for **Asynchronous digital sample-rate converter** • • • 5,479,048 to Kevin Yallup and Oliver Creighton for **Integrated circuit chip supported by a handle wafer and provided with means to maintain the handle wafer potential at a desired level** • • • 5,477,078 to David F. Beigel, William A. Krieger, and Susan L. Feindt for **Integrated circuit (IC) with a two-terminal diode device to protect metal-oxide-metal capacitors from ESD damage** • • • 5,479,119 to Thomas E. Tice, David T. Crook, Kevin M. Kattmann, and Charles D. Lane for **High speed active overvoltage detection and protection for overvoltage-sensitive circuits.**

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